Development of a low noise integrated readout electronic for pixel detectors in CMOS technology for a Compton camera

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by
Joachim Hausmann

Abstract: Semiconductor detectors are very popular, particularly for their good energy resolution and their easy handling. Combined with a two dimensional spatial resolution such a detector is predestined to realise an active collimation in a Compton camera for medical applications. To measure the deposited energy in each channel (pixel), a self-triggering integrated electronic has been developed, which is directly bonded on top of the detector. The design of the low noise readout electronic ('Ramses') for a 32 x 32 matrix of 150 µm x 150 µm pixels, the layout and measurements are presented. Closest attention is paid to silicon detectors, which are favoured for Compton scattering with regard to Doppler effect. Nevertheless the electronic chip is also designed to measure the energy deposited by photo absorption in a detector material with higher atomic numbers (GaAs, CdTe).

Abstraktum: Halbleiterdetektoren sind weit verbreitet, insbesondere auf Grund ihrer hervorragenden Energieauflösung und einfachen Handhabbarkeit. Gepaart mit einer zweidimensionalen Ortsauflösung sind sie insbesondere prädestiniert, eine aktive Kollimation, wie beispielsweise innerhalb einer Compton-Kamera zur medizinischen Diagnostik, zu implementieren. Um die Energieinformation eines jeden Kanals (Pixels) zu gewinnen, ist eine selbsttriggernde, integrierte Elektronik entwickelt worden, die direkt auf den Detektor aufgebracht wird. Im folgenden werden sowohl die Konzepte der rauscharmen analogen Pixelmatrix-Signalverarbeitungselektronik aus Siegen ('Ramses') für eine 32 x 32 Matrix, basierend auf 150 µm x 150 µm großen Pixeln, als auch deren layouttechnische Umsetzung sowie Messungen präsentiert. Das Hauptaugenmerk richtet sich dabei auf Siliziumdetektoren, die hinsichtlich des Doppler-Effektes das Material der Wahl für den Comptoneffekt darstellen. Der gleiche Elektronikchip ist auch geeignet, die Energie bei Photoabsorption in Detektormaterialien mit höherer Kernladungszahl (GaAs, CdTe) zu bestimmen.

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1 Introduction

The progress in nuclear and later on in elementary particle physics is closely connected with the advances in detector physics and technology. The interaction of charged particles and radiation with matter is used for detection. The most widely used materials for this purpose are gases (e. g. in the Geiger-Müller counter), but also liquids (e. g. Argon) and even solid materials (semiconductor detectors) are common. Particularly silicon is widely spread, since it is well understood, generates a natural oxide (SiO_2) with nearly the same lattice parameter, which is important to form several interesting structures (e. g. MOSFETs), and last but not least is relatively cheap.

The development of position-sensitive semiconductors has been pushed by the requirements of experimental particle physics to measure particle tracks to a precision of several µm. At the same time these detectors have to operate at high rates (several MHz). For spectroscopy energy resolving detectors (e. g. high purity Ge-detectors) are required.

In the meantime a semiconductor detector, the famous charged coupled device (CCD), has found its way to consumer's electronics like video cameras, digital cameras or scanners. Spin-offs are also used in biological, chemical and medical applications. The idea of a Compton camera, an imaging system for X-rays with active collimation, based on semiconductor pixel detectors is the genesis of this thesis. Highly integrated CMOS (complementary metal-oxide-semiconductor) chips offer the possibility for a multichannel low noise electronics for an energy resolved readout of pixelated semiconductor detectors. In this thesis the implementation of readout electronics on an integrated circuit is investigated and presented.

The present text is divided into eight chapters. The second chapter, which follows this short introduction, gives a brief overview of standard methods for medical imaging with radioactive isotopes and introduces the idea of the Compton camera. For this purpose the interaction of photons with matter is briefly reviewed. Chapter 3 describes the principle of a semiconductor detector, beginning with an introduction to semiconductors, reviewing the pn-junction and important aspects of detector materials. This chapter ends up in the presentation of segmented detectors and different bonding techniques.

The quintessence of this thesis is formed by chapter 4 to 6. The fourth chapter describes the implemented readout blocks of the electronic chip. Primarily the concept of detector referred equivalent noise charge is introduced and the pixel electronic is discussed. The peripheral logic for data reduction and off-chip communication will be presented. In chapter 5 the test system environment is introduced and the corresponding measurements are subsumed in chapter 6.

In chapter 7 conclusions from the considerations and results of this work are drawn. An outlook towards possible further improvements is given.

Chapter 8 reviews important fundamentals of CMOS: The basic structure of a MOSFET (metal-oxide-semiconductor field-effect transistor) together with the most relevant equations are given. General problems (latch-up) and handling procedures of

CMOS chips are discussed. Finally basic circuits, both analog and digital, and the origins of noise are reviewed. The chapter is closed by some data sheets and layouts of the three revisions of the chip and by a table of often used physical constants.

2 Medical Imaging with Radioactive Isotopes

2.1 Interaction of Photons with Matter

X-rays and γ-rays are two synonyms for photons[1] (electromagnetic quanta) with energies above some 100 eV.

To detect a photon, at least part of its energy must be transferred to a charged particle, which is subsequently detected by ionisation. The interaction of photons with matter is subdivided into three effects: photoelectric effect, Compton effect and pair production. [Eic 79], [Gru 93], [Leo 94], [Kno 79]

2.1.1 The Photoelectric Effect

The complete energy of an incident photon is absorbed by an electron bound to an atom (free electrons cannot absorb this energy for reasons of conservation of momentum). The cross section for the absorption of a photon in the K-shell is particularly high, because of the nearby nucleus.

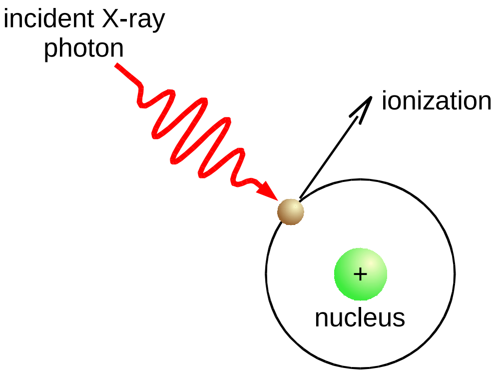

Figure 2.1 Photo ionisation

For energies above the K-edge[2] the cross section is approximately inversely proportional to ${E_\gamma}^{7/2}$ and proportional to Z^n, where n varies from 4 at E_γ=100 keV to n=4.6 at E_γ=2 MeV [Mar 69, Gru 93].

The photoelectric effect is the dominant interaction of photons with matter for those photons, whose energy falls approximately in the range 1 keV < E_γ < 50 keV. The upper limit depends on the used absorber and is given for silicon. For higher Z the photoelectric effect dominates up to 500 keV.

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[1] While photons emitted from atomic shells and bremsstrahlung are usually called X-rays, the photons emitted from atomic nuclei and annihilation radiation are called γ-rays. As for the interaction with matter the origin of the photons plays no role, the terms are used in a non-specific way in this thesis.

[2] The K-edge for silicon lies at 1.84 keV, for lead at 88.0 keV.

In consequence of the photo effect, the originated vacation will be filled by an electron of the outer shell. The excessive energy is emitted as a photon or transferred to an electron of an outer shell, which thus can escape from the atom (Auger electron). In silicon a vacation in the K-shell leads to an Auger process in 95 % of the cases and only in 5 % of the cases to an emission of a 1.74 keV X-ray. However in materials with higher Z this ratio reverses.

2.1.2 Pair Production

For the production of a positron/electron pair in the coulomb-field of a nucleus a minimum energy of twice the rest mass (511 keV) of an electron is needed. As the energy of photons used in medical application is less than 511 keV pair production does not act a role.

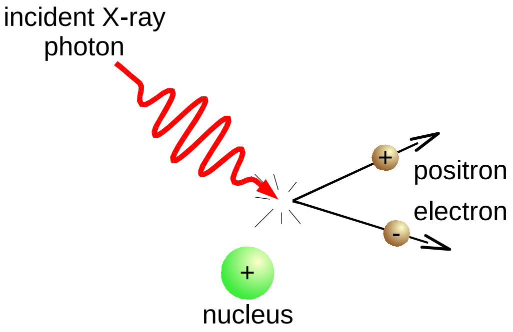

Figure 2.2 Pair production

2.1.3 The Compton Effect

Another possible outcome of an interaction between an incident photon and an electron in the target material is an elastic collision in the classical billiard ball sense. This is known as the Compton effect in honour of Arthur Compton, who discovered it in 1923 (see [For 74] pp 1068-71). In the simplest case, a free electron at rest is struck by a photon that scatters off at some angle to its original path. By the conservation of momentum and energy, the electron must recoil in a specific direction, with a specific energy. This energy must be provided by a reduction in the energy of the photon (increase in its wavelength).

The change in wavelength of the scattered photon is given by

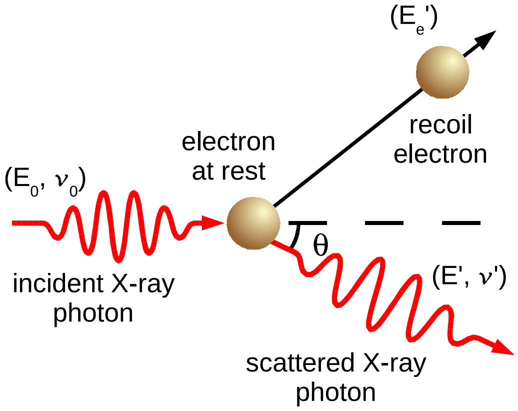

Figure 2.3 Compton effect at a free electron

$$\frac{c}{\nu'}-\frac{c}{\nu_0}=\lambda'-\lambda_0=\frac{h}{m_e c}(1-\cos\theta) \tag{2.1}$$

where θ is the scattering angle of the scattered photon. The energy E'_e transferred to the recoil electron results in the energy loss of the X-ray photon:

$$E'_e=h(\nu_0-\nu')=h\nu_0\frac{\alpha(1-\cos\theta)}{1+\alpha(1-\cos\theta)} \tag{2.2}$$

with

$$\alpha=\frac{h\nu_0}{m_e c^2} \tag{2.3}$$

The scattering angle is reconstructed by

$$1-\cos\theta=\frac{E'_e}{\alpha(h\nu_0-E'_e)} \tag{2.4}$$

In practice, of course, available electrons are usually bound to atoms, so that the approximation of a free, stationary electron is that the photon energy greatly exceeds the binding energy of the electron. For X-ray photons and valence electrons this is certainly reasonable. As [Kid 89] state, for $E_\gamma = h\nu \ll m_e c^2$, the Compton electron recoils approximately in the direction of the electric field vector of the incident light and Compton scattering merges smoothly into classical Thomson scattering in the limit of low frequency.

The probability of Compton scattering is typically small, but at energies around 1 MeV it is usually the most common interaction. The probability of the photoelectric effect declines with increasing photon energy. Pair production does not typically dominate until about 10 MeV.

One may readily view Compton scattering in terms of the energy loss, ΔE, or the wavelength increase $\Delta\lambda$ as a function of θ, the angle between the initial and final photon directions. Examination of the algebra leads to the intuitively reasonable conclusion that the maximum momentum, and hence also the maximum energy, will be transferred from the photon to the target particle when the final photon travels in the opposite direction to the incident photon (θ=180°).

The differential cross-section for the Compton effect is given by the Klein-Nishina formula [Leo 94]. For studying the energy deposition in a detector the energy distribution of the Compton electrons is an important function (derived from the Klein-Nishina formula), given by

$$\frac{d\sigma}{dE'_e}=\frac{\pi r_e^2}{m_e c^2 \alpha^2}\left[2+\frac{s^2}{\alpha^2(1-s)^2}+\frac{s}{1-s}\left(s-\frac{2}{\alpha}\right)\right] \tag{2.5}$$

where $s=E'_e/E_\gamma$ and the classical electron radius r_e=2.818 fm.

From equation 2.2 the maximum recoil energy is derived:

$$E'^{max}_e=h\nu_0\frac{2\alpha}{1+2\alpha} \tag{2.6}$$

In the energy spectrum of the Compton recoil electron this maximum energy is known as the Compton edge.

2.2 Single Photon Emission Computed Tomography (SPECT)

Single Photon Emission Computed Tomography is a technique that uses a computer for reconstruction of the distribution of a single gamma emitting nuclide[3] detected by a rotating gamma camera. Its essential goal is enhancement of the image detectability and the extraction of quantitative data from a true three dimensional distribution of a radioactive tagged structure (or radioactivity) in space. Any conventional (planar) imaging technique is restricted mainly to the visualisation of objects in three dimensional space by two dimensional projections. Multiple views of an object from different angles are required to appreciate its three dimensional structure. These separate views are usually called projections. A complete set of projections potentially permits a complete reconstruction of object structure in three dimensions.

To record a projection, a gamma camera, also known as Anger[4] camera, is used (Figure 2.4). It is based on a scintillator, which converts γ-rays passing the collimator to light, which is subsequently detected by photomultipliers. The collimator – in its simplest version a lead plate with several parallel pinholes – selects the direction of the incident γ-rays as it absorbs transversely impinging radiation.

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[3] The widely used ^{99m}Tc, which emits single 140 keV gamma photons, is an example. Others are ^{133}Xe and ^{123}I

[4] The scintillation camera was invented in 1958 by Hal Anger

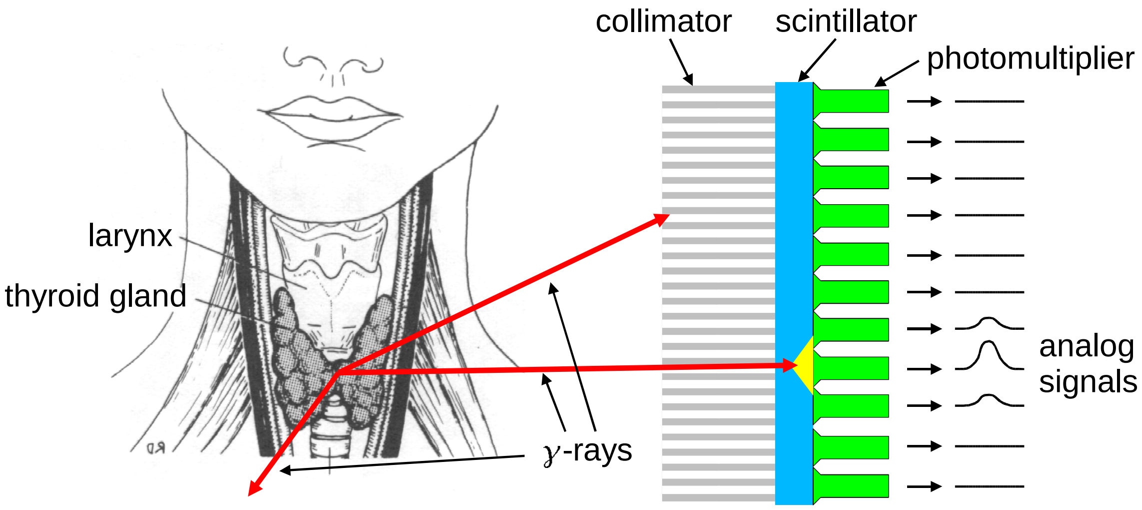

Figure 2.4 Principle of an Anger camera: Only those rays passing the collimator are converted to light and are seen by the photomultiplier

2.3 Positron Emission Tomography (PET)

A positron emitter is an unstable isotope, which decays to a stable state by ejecting a positron from its nucleus. The positron, depending upon its energy, travels a small distance in tissue, typically 1...2 mm, before it annihilates with a surrounding electron. Two gamma rays are emitted in diametric opposition to each other. To enrich the region of interest with a positron emitter, a dedicated radioactive substance is injected into the patient.

The electronics and detectors of the PET scanner are designed to record only those gamma rays, which occur simultaneously[5] at opposite detectors.

In a PET scan the patient incorporating a radioactive substance is placed on a flat table that moves in increments through a donut shaped housing. This housing contains the circular gamma ray detector array (Figure 2.5), which has a series of scintillation crystals, each connected to a photomultiplier tube (similar to SPECT). The crystals convert the gamma rays, emitted from the patient, to photons of light, and the photomultiplier tubes convert and amplify the photons to electrical signals. These electrical signals are then processed by a computer to generate images. The table is then moved, and the process is repeated, resulting in a series of thin slice images of the body over the region of interest (e. g. brain, breast, liver). These thin slice images are assembled into a three dimensional representation of the patient's body.

However, there are few PET centres in the country, because they must be located near a particle accelerator device that produces the short-lived radioisotopes used in this technique.

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[5] Simultaneously means within a certain time window of a few nanoseconds

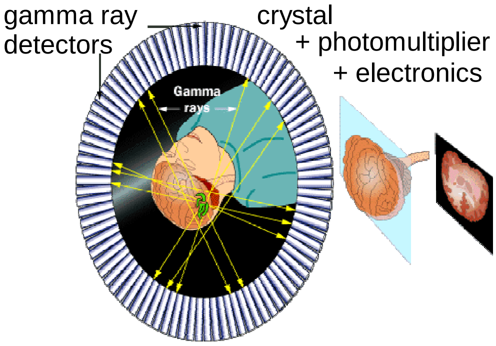

Figure 2.5 PET scanner

2.4 The Compton Camera

2.4.1 The Working Principle of a Compton Camera

The attraction of Compton cameras lies in their potential to achieve imaging performance that is better than that of Anger cameras. Instead of mechanical collimation, Compton cameras utilise the Compton scattering interaction to localise the original directions of gamma rays emitted from source distributions. This localisation is based on the well-known equation (see section 2.1.3) that relates the angle of scattering to the energies of a gamma ray before and after Compton interaction with a free electron at rest:

In principal an incident X-ray photon is non-ambiguously reconstructed, if the direction of the scattered X-ray and the recoil electron is traced. This is done in Compton cameras for astronomy (e. g. MEGA-project (Medium Energy Gamma-Ray Astronomy) of the MPE[6]).

In medical applications the γ-energy is comparatively low, which makes it on the one hand difficult to trace the electron as its energy is also likewise low. On the other hand it is easier to measure the energy of the recoil electron near the scattering point by means of a pixelated detector, because the range of the low energetic electron is small (see Figure 2.6).

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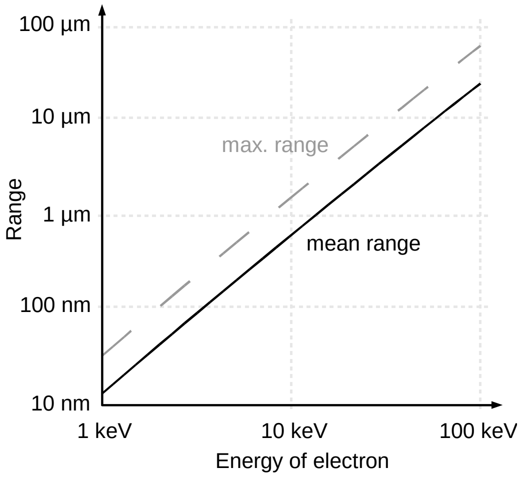

Figure 2.6 Estimated mean and maximum range of electrons in silicon [Ove 98]

The idea to realise a Compton camera is based on a pixelated detector, in which the Compton scattering takes place and is localised by measuring the energy transferred to the recoil electron. If a semiconductor is used as a Compton detector, the range of an electron of several keV is lower than a µm as shown in Figure 2.6 for silicon. A subsequent photoelectric absorption of the scattered photon in a second pixelated detector resolves the direction of the scattered photon as shown in Figure 2.7.

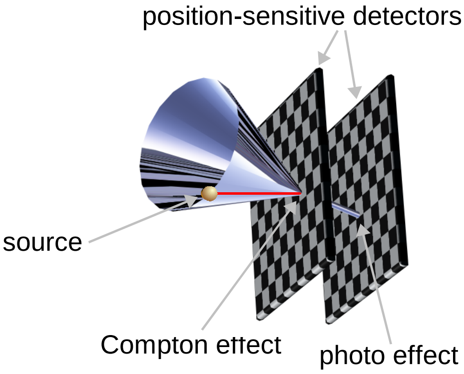

Figure 2.7 Reconstruction of the incident photon: limited to a surface of a cone

From the measured energy of the recoil electron (E_e') the scattering angle (θ) is derived (see equation 2.4). Together with the position of the Compton scattering and the direction of the scattered photon the incident photon direction is limited to the surface of a cone. The superposition of some cones from the same point source resolves its three dimensional position (Figure 2.8).

The resolution of the energy of the recoil electron translates to an uncertainty in the scattering angle. A simple estimation for a scattering angle of $\theta=90°$ and an uncertainty of $\Delta\theta=1°$ leads to an energy resolution of the recoil electron of $\Delta T=23$

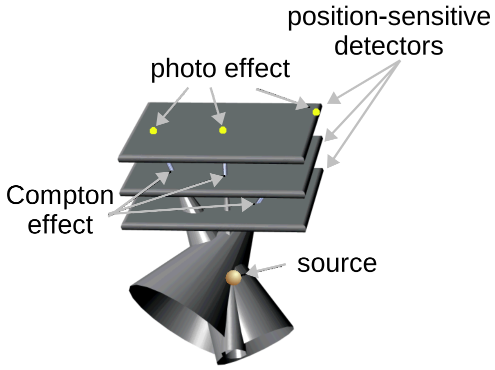

Figure 2.8 Superposition of three cones

eV. The dedicated readout electronic has to be designed to achieve an adequate low noise.

Doppler Effect

In the derivation of the Compton effect the recoil electron before the interaction is assumed as free and at rest. The reality, however, is that an incident gamma ray interacts with moving electrons that are bound to atoms in the scatter detector (Fig. 2.9). Therefore, the kinematics of a scattered gamma ray depends on the state (the momentum and binding energy) of the struck electron. A serious consequence of the bound Compton scattering is Doppler broadening: for each scattering angle, there will be a distribution of energies deposited in the scatter detector, instead of a single, unique energy. A complete theoretical treatment of Compton scattering is given in [Wil 77].

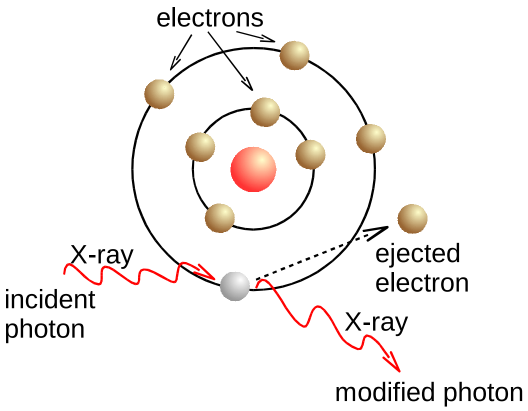

Figure 2.9 Compton scattering at an electron bound to an atom

The geometry of a Compton scattering process, in which the electron is not assumed as at rest, is shown in Figure 2.10.

The scattering vector $\vec{q}$ is the difference of the wave vector of the photon after collision ($|\vec{k}'| = \frac{\omega'}{c} = \frac{E'}{\hbar c}$) and before collision ($|\vec{k}| = \frac{\omega}{c} = \frac{E}{\hbar c}$). The electron

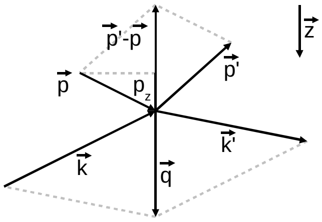

Figure 2.10 Geometry of Compton scattering process

momentum is given before ($\vec{p}$) and after collision ($\vec{p}\,'$). The projection of $\vec{p}$ onto the scattering vector $\vec{q}$ is denoted as p_z. It is given by [Eva 99]:

$$p_z = \frac{\hbar\,\omega\,\omega'(1-\cos\theta)-m_e c^2(\omega-\omega')}{\sqrt{\omega^2+\omega'^2-2\,\omega\,\omega'\cos\theta}} = \frac{E\,E'(1-\cos\theta)-m_e c^2(E-E')}{\sqrt{E^2+E'^2-2\,E\,E'\cos\theta}} \tag{2.7}$$

This equation is valid under a set of conditions known as the impulse approximation[7], which requires that the recoil electron energy is much greater than its binding energy. This means that it does not satisfactorily describe small-angle scattering from inner-shell electrons.

The intensity of scattered photons at any energy E' will be proportional to the probability of observing the corresponding momentum component p_z. That probability is described by the scattering material's Compton profile $J(p_z)$. The Compton profile for silicon has been measured using the Compton effect [Ree 72] and is shown in Figure 2.11. It is compounded of a relatively narrow peak due to the four electrons in the outer shell (low binding energy of 0.4 keV) and a broader distribution from the core electrons (large binding energy of 2.3 keV). The momentum transfer p_z is given in atomic units (1 a. u.$=\alpha mc=3.7$ keV/c).

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[7] The outgoing electron is treated as a plane wave so that the target potential is assumed to be constant during the collision.

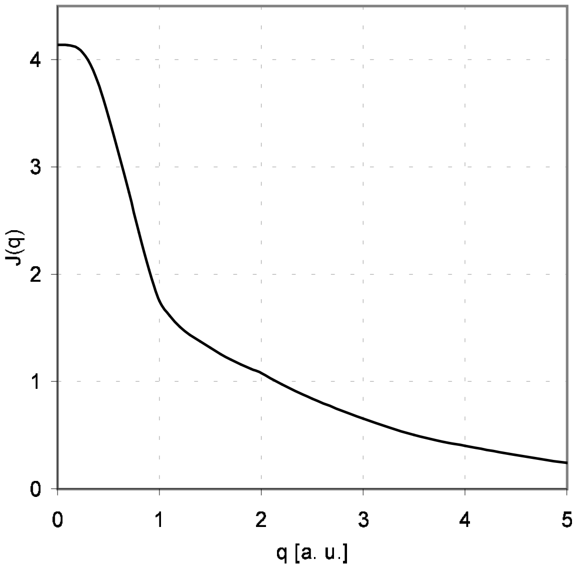

Figure 2.11 Measured Compton profile in silicon [Ree 72]

Solving equation 2.7 for 1−cos θ yields ($\hbar = c = 1$):

$$1-\cos\theta = m\left(\frac{1}{E'}-\frac{1}{E}\right)+\underbrace{\frac{p_z q}{E E'}}_{\Delta(\cos\theta)} \quad \text{with } q=\left|\vec{k}'-\vec{k}\right| \tag{2.8}$$

With the change $\Delta(\cos\theta)$ due to the electron motion, the uncertainty $\Delta\theta$ is given by

$$\Delta\theta = \frac{\Delta(\cos\theta)}{\sin\theta} = \frac{p_z}{E} f(\theta, E) \tag{2.9}$$

The function $f(\theta, E)$ is plotted for different energies in Figure 2.12. It varies very little in $0° \leq \theta \leq 110°$. The smearing $\Delta\theta$ of the scattering angle due to the Doppler-effect is therefore proportional to $1/E_\gamma$, i. e. most prominent at low energies:

$$\Delta\theta_{FWHM} \approx \left(\frac{p_z}{E}\right)_{FWHM} \approx \left(\frac{6.5\,\text{keV}}{E\,[\text{keV}]}\right)_{FWHM} \tag{2.10}$$

For an initial photon energy of 100 keV the uncertainty is $\theta \approx 65$ mrad$\approx 3.7°$. Therefore the lateral resolution of a 2 cm distant source is limited to 1.3 mm by Doppler broadening. To obtain an useful spatial resolution, a Compton camera therefore needs γ-sources of at least 100 keV.

It is also clear that the low atomic weight of silicon is an advantage, since the fraction of outer shell electrons is higher than in heavy nuclei. Silicon is therefore the natural choice for a Compton scattering detector.

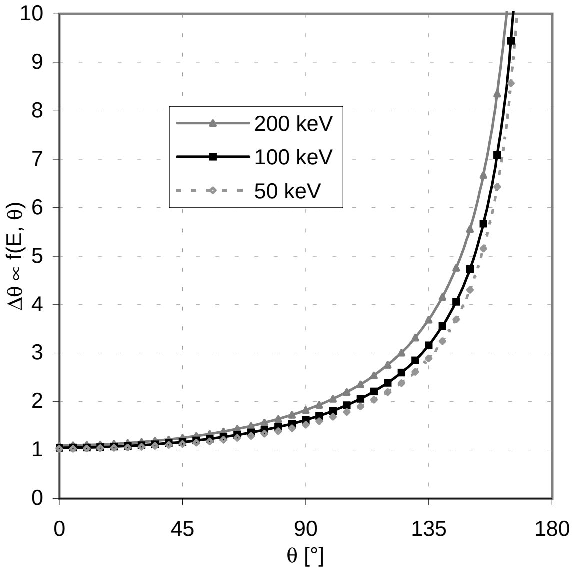

Figure 2.12 Function to characterise the uncertainty of the scattering angle θ

3 Principle of a Semiconductor Detector

This chapter shall give an introduction to semiconductor detectors. Starting with a short repetition of the properties of semiconductors, the pn-junction will be discussed afterwards. Aspects of the use of semiconductors as radiation detectors are given and some important characteristics are discussed. The chapter ends with the transition from a single non-segmented detector to strip- and pixel-detectors respectively, which permit a spatial resolution of the radiation interaction point.

3.1 Semiconductors

Materials can be categorised into conductors, semiconductors or insulators by their ability to conduct current. The band theory of materials explains qualitatively the difference between these types of materials. Electrons occupy energy levels from the lowest energies upwards. However, some energy levels are forbidden because of the wave like properties of atoms in the material. The allowed energy levels tend to form bands. The highest filled level at T=0 K is known as the valence band. Electrons in the valence band do not participate in the conduction process. The first unfilled level above the valence band is known as the conduction band. In metals, there is no forbidden gap; the conduction band and the valence band overlap, allowing free electrons to participate in the conduction process. Insulators have an energy gap that is far greater (>3 eV) than the thermal energy of the electron, while the energy gap of semiconductor materials is typically around 1 eV (at T=300 K: E_g(silicon)=1.12 eV, E_g(germanium)=0.66 eV [Sze 81]).

Intrinsic semiconductors are essentially pure semiconductor materials. The semiconductor material structure should contain no impurity atoms. Both elemental and compound semiconductors can be intrinsic semiconductors. At room temperature, the thermal energy of the atoms may allow a small number of the electrons to participate in the conduction process. Unlike metals, the resistance of semiconductor material decreases with temperature. As the temperature increases, the thermal energy of the valence electrons increases, allowing more of them to breach the energy gap into the conduction band. When an electron gains enough energy to escape the electrostatic attraction of the atom, it leaves behind a vacancy, which may be filled by another electron. The vacancy produced can be thought of as a second carrier of positive charge. It is known as a hole. While electrons flow through the semiconductor, holes flow in the opposite direction. If there are n free electrons in an intrinsic semiconductor, then there must also be n holes. Holes and electrons created in this way are known as intrinsic charge carriers. The carrier concentration or charge density defines the number of charge carriers per unit volume. This relationship is expressed as $n=p$ where n is the number of electrons and p the number of holes per unit volume. The variation in the energy gap between different semiconductor materials means that the intrinsic carrier concentration at a given temperature also varies.

An extrinsic semiconductor is formed from an intrinsic semiconductor by adding impurity atoms to the crystal in a process known as doping. To take the most simple example, consider silicon. Since silicon belongs to group IV of the periodic table, it has for valence electrons. In the crystal form, each atom shares an electron with each neighbouring atom. In this state it is an intrinsic semiconductor. Boron, aluminium, indium and gallium have three electrons in the valence band. When a small proportion (less than 1 in 10^6) of these atoms is incorporated into the crystal the dopant atom has an insufficient number of bonds to share bonds with the surrounding silicon atoms. One of the silicon atoms has a vacancy for an electron. It creates a hole that contributes to the conduction process at all temperatures. Dopants that create holes in this manner are known as acceptors. This type of extrinsic semiconductor is known as p-type as it creates positive charge carriers. Elements that belong to group V of the periodic table such as arsenic, phosphorus and antimony have an extra electron in the valence band. When added as a dopant to intrinsic silicon, the dopant atom contributes an additional electron to the crystal. Dopants that add electrons to the crystal are known as donors and the semiconductor material is said to be n-type.

3.2 The pn-Junction

Most semiconductor devices are based on the properties of the interface between a p-type semiconductor and an n-type semiconductor, a so-called pn-junction. For illustration purposes this junction is formed by the juxtaposition of both types of doped semiconductors, in practice special techniques must be used to realise such a junction [Leo 94].

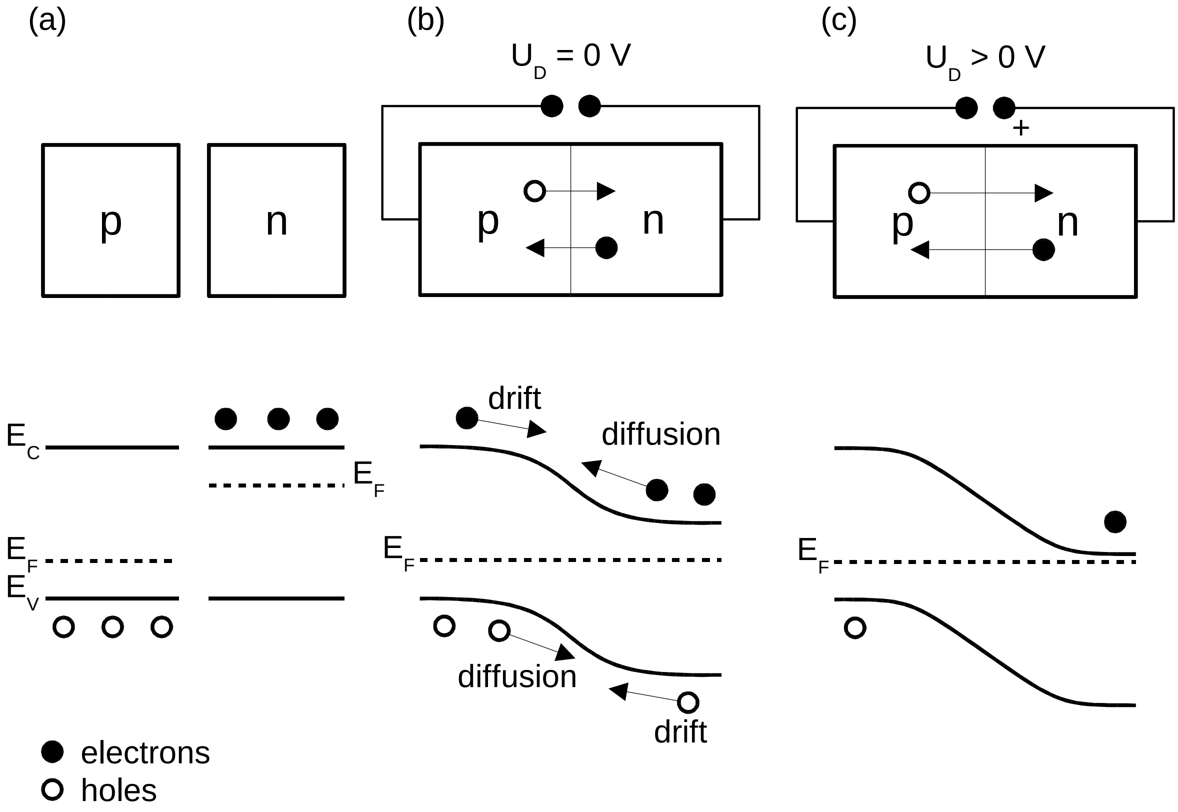

Figure 3.1 pn-junction of a semiconductor diode with equal doping level in the p-type and n-type zone. The energy levels are shown for a) the p-type and n-type zones separated, b) a pn-diode without an external voltage applied, c) a reversed biased pn-diode.

Figure 3.1 shows the energy levels of a p-type semiconductor and an n-type semiconductor respectively. Impurity levels shift the Fermi level in the p-type towards the valence band, in the n-type towards the conducting band. In the thermodynamic equilibrium both Fermi levels are equalised. Because of the difference in the concentration of electrons and holes between the two materials, there is an initial diffusion of holes towards the n-region and a similar diffusion of electrons towards the p-region. So diffusing electrons fill up holes in the p-region while diffusing holes capture electrons on the n-side. Recalling that the n- and p-structures are initially neutral, this recombination of electrons and holes also causes a charge build-up to occur on either side of the junction. Since the p-region is injected by extra electrons it thus becomes negative while the n-region becomes positive. This creates an electric field gradient across the junction, which eventually stops the diffusion process leaving a region of immobile space charge. The charge density and the corresponding electric field profile are schematically diagrammed in Figure 3.2. The electric field causes a potential difference across the junction known as the contact potential. The energy band structure is thus deformed as shown in Figure 3.1. The region of changing potential is known as the depletion zone or space charge region and has the special property of being devoid of all mobile charge carriers: Any electron or hole created or entering into this zone will be swept out by the electric field. This characteristic of the depletion zone is particularly attractive for radiation detection. Ionising radiation entering this zone will liberate electron-hole pairs, which are then swept out by the electric field. If electrical contacts are placed on either end of the junction device, a current signal proportional to the ionisation will then be detected. The analogy to an ionising chamber thus becomes apparent.

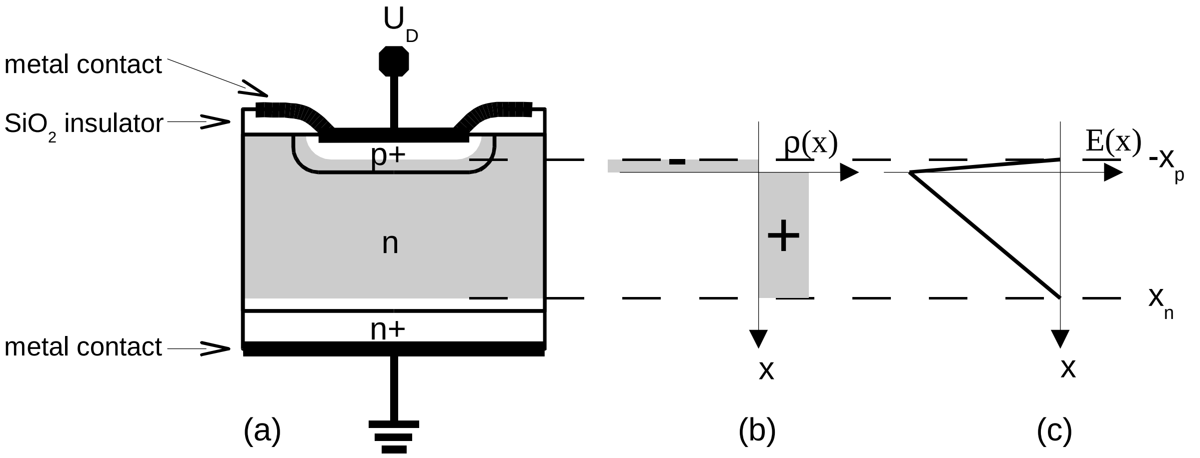

Figure 3.2 a) Realisation of a pn-photodiode, b) simplified charge distribution in the depletion zone, c) electric field intensity

3.3 Semiconductor Detectors

The action of a nuclear particle in a semiconductor detector is to raise electrons from the valence band to the conduction band by supplying an energy of E_g (the energy gap across the forbidden band). On a doped semiconductor material only host atoms are considered to be affected, since the fraction of impurity atoms is always negligible in this context. Thus equal number of electrons and holes are produced. These may recombine with one another, be trapped at 'trapping centres' or be collected by the electrodes of the detector. Direct recombination is rare, and it is the concentration of recombination traps, which critically determines the lifetime of the carriers. Other types of trapping can occur where the carrier is trapped for a long period compared to the collection time, but is eventually released. This is often made worse by an additional effect, since the trapped carriers constitute a space charge and, to maintain electro-neutrality, an associated number of carriers of the opposite sign are retained in the material. Since these are free to move, they give an increased conductivity during the trapping period.

Compared with competing techniques, the use of semiconductor detectors often provides advantages in a number of key areas. These include exceptionally good energy resolution, good stability and freedom from drift, excellent timing characteristics, very thin entrance windows, and simplicity of operation.

3.3.1 Semiconductor Materials used for Radiation Detection

Although it may appear at first sight that many insulating or semiconducting materials may be used to form the basis of a solid state ionisation chamber, that is not the case for a number of reasons. In most solids the electrons and holes would be trapped very quickly or would recombine at defect centres, so that they could only migrate a negligible distance under the influence of the biasing field, and induce a negligible voltage change on the electrodes. Even if this were not the case, the conductivity of many materials is too high, so that the leakage current due to the biasing voltage would swamp any signals present. These two considerations alone limit the choice of materials to those available in high purity.

In general, the main properties required for a semiconductor detector material are:

a) high atomic number *(Z)* for efficient radiation interaction

b) small energy gap E_g to generate a large number of electron-hole pairs by the incident nuclear particle to improve energy resolution

c) large enough bandgap (or low quiescent carrier concentration) for high resistivity and low leakage current

d) high mobilities of holes and electrons and long carrier lifetime for efficient collection and a fast rise time of the signal

e) freedom from delayed trapping to give a fast rise time and freedom from space charge effects

f) high purity, homogeneous, defect-free material with acceptable cross-sectional area and thickness

g) electrodes that produce no defects, impurities or barriers to the charge collection process

3.3.2 Ionisation Energy and the Fano Factor

For detector applications the average energy expended by the primary charged particle to produce one electron-hole pair is of practical interest. This quantity (ionisation energy) is experimentally observed to be largely independent of both the energy and type of the incident radiation. The dominant advantage of semiconductor detectors lies in the smallness of this energy (typically some eV, which is about ten times smaller than in gas-filled detectors).

It is possible to view the effect of the ionisation energy in two extreme cases. In the first we may assume that the creation of each ion pair has a constant probability, independent of the creation of other ion pairs. For such a random phenomenon, a Poisson distribution would govern the total number of ion pairs; and if the mean number of ion pairs were N, the standard deviation would be $\sqrt{N}$. At the second extreme, the part of the particle energy producing ionisation would be exactly apportioned in the production of ion pairs and the standard deviation would be zero. The true state of affairs lies somewhere between the two extremes and the standard deviation may be written as $\sqrt{FN}$, where F is the so-called Fano factor. The Fano factor for silicon is 0.115, for germanium 0.13 and for diamond 0.08. [Ali 80]

3.3.3 pn-Junction Detectors

A pn-junction detector is a reverse-biased diode. The main characteristics of interest for its use as a radiation detector are its leakage current and its capacitance. When a pn-junction is reverse-biased, there's a small current flow (leakage current), related to the bulk volume and surface of the detector. Bulk leakage currents arising internally within the volume of the detector are caused by either of two mechanisms: minority carriers current and thermal generation of electron-hole pairs within the depleted region. The latter is the more important of the two processes. Surface leakage effects take place at the edges of the junction, where relatively large voltage gradients must be supported over small distances.

The detector capacitance depends on the detector dimensions. The p^+ contact carries a negative space charge and is connected to the cathode of a high voltage supply. The n^+ contact carries a positive space charge and is connected to the anode. In the large intrinsic region, an electric field exists due to both the space charges and the applied reversed bias, V. This capacitor has a momentary leak current as a result of the interaction with the ionising particles. The magnitude at each moment of this current through the detector, i, is calculated as follows: The ionising radiation creates N charge carriers with charge q at a certain place in the active detector volume. This charge $N \cdot q$ starts to flow under the influence of the electric field E at this place, resulting in a current of $i = NqEv/V$, with v the velocity of the charges at the place.

3.3.4 Some Characteristics of Semiconductor Radiation Detectors

A few characteristics of semiconductor radiation detectors are detector efficiency and resolution, timing resolution, dead layer and changes with bias voltages.

The detector efficiency is a measure of the probability that particles of a certain energy will be absorbed in the sensitive area of the detector. This probability depends basically on a geometrical and an intrinsic factor. The geometrical factor accounts for the fact that the probability of a particle to impinge on the detector depends on the relative positions of both the source and the detector. The intrinsic factor accounts for the probability of total absorption of the energy in the active volume of the detector. A characteristic energy-dependant efficiency is found for each detector.

The system resolution is a measure of its capability to distinguish two energetically close lying events from each other. It is expressed as the full width at half maximum (FWHM) and it is expressed in energy units (keV or eV).

The timing resolution of the detector is greatly dependant on the charge collection time. The charge collection time depends on the detector geometry, depletion voltage and the location of the interaction within the detector. The measured timing resolution depends on many parameters: the detector dimensions, geometry and field distribution, the speed of the preamplifier, the timing modules used as well as their adjustments, the source and its position and the energy range of the coincident gamma rays. The actual rise-time observed from a detector-preamplifier combination is influenced by the detector and the preamplifier properties.

When a heavy charged particle or other weakly penetrating radiation is involved, the energy loss that may take place before the particle reaches the active volume of the detector can be significant. Because the thickness of the dead layer includes not only the metallic electrode but also an indeterminate thickness of silicon immediately beneath the electrode, in which charge collection is inefficient, the dead layer can be a function of the applied voltage. Its effective thickness must often be measured directly by the user if accurate compensation has to be made.

When the bias voltage and electric field are low, the pulse height from radiation that is fully stopped within the depletion layer continues to rise with applied voltage. This variation is caused by the incomplete collection of charge carriers because of trapping or recombination along the track of the incident particle. The fraction that escapes collection will decrease as the electric field is increased.

3.3.5 Segmented Sensors

With a pn-junction detector radiation can be detected. In order to obtain a spatial information about the position, where the radiation is detected, the detector must be segmented. Parallel strips of a p^+-implantation in an n-bulk (or vice versa) allow an one dimensional resolution (see Figure 3.3). Additional perpendicular n^+-strips on the opposite side of the detector gives a two dimensional resolution[8].

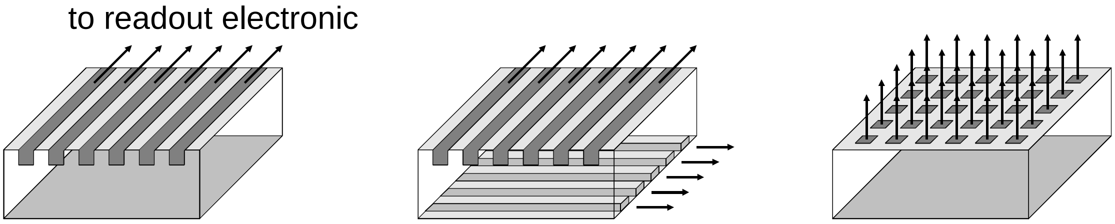

Figure 3.3 Segmentation of semiconductor sensors: single-sided strip, double-sided strip, single-sided pixel

In a double-sided strip detector simultaneously[9] occurring multiple hits causes ambiguities in the reconstruction. Those ambiguities do not exist in pixel detectors. The smaller pixel area results in a lower detector capacity and consequently in a lower noise [Kru 91]. A great challenge of the segmentation of detectors is the increasing number of readout channels with subtler granularity. For a given granularity the number of readout channels of strip detectors rises linear with the perimeter of the sensitive area, in pixel detectors even quadratic. The large number of readout channels together with a small pitch of the strips for a high spatial resolution requires a dedicated integrated readout chip.

As the connection between strip detector and readout electronic can still be established in a two dimensional way, i. e. the readout electronic is located beside the sensor and connected via wire bonds, the pixel detector needs a three dimensional connection, i. e. a headlong interface of the sensor and the electronic (bump bonding, see next subsection).

To develop a readout electronic, basically three parameters of the detector have to be known:

- The polarity of the detector, i. e. the doping of the segmented structure, which will be connected to the readout electronics. The readout electronics for the Compton camera was designed for p^+ in n-detectors. This means that the pixel structure is

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[8] Special techniques have to be applied to isolate adjacent n^+-strips; also the detector has to be fully depleted to avoid a short between two n^+-strips via the n-substrate.

[9] The term "simultaneously" depends on the dead-time of the detector and readout speed of the electronic. The dead-time limits also the counting rate of the system.

p^+ doped and connected to the more negative voltage compared to the n-side (reverse bias). Therefore holes will be collected by the readout electronic.

- To achieve an optimal signal to noise ratio, the detector capacitance for capacitive matching must be known. The capacitance of a semiconductor depends on the thickness of the depletion zone and therefore on the detector bias voltage. When a reversed bias voltage V_{bias} is applied to the junction, the depletion zone extends almost entirely into the n-bulk. Its thickness is given by [Leo 94]

$$d \approx \sqrt{\frac{2\varepsilon_{Si}}{q} \frac{V_0 + V_{bias}}{N_D}} = \sqrt{2\varepsilon_{Si} \rho_n \mu_e (V_0 + V_{bias})} \tag{3.1}$$

  where V_0 denotes the diffusion voltage (contact potential), N_D the concentration of donors in the n-region, ε_{Si} the dielectric constant for silicon ($\varepsilon_{Si}=11.7 \cdot 8.85 \cdot 10^{-12}$ As/Vm), q the elementary charge, ρ_n the resistivity of the n-region and μ_e the mobility of electrons.

  For a planar geometry (area A, distance d, permittivity $\varepsilon=\varepsilon_r \cdot \varepsilon_0$), the capacitance is given by

$$C = \varepsilon \frac{A}{d} \tag{3.2}$$

  As the pixel structure often is very small, the thickness of the capacitance is at least of the order of the lateral dimensions. Therefore the ideal case of equation 3.2 is not achieve due to edge effects and additional capacitances to the neighbouring pixels. A pixel of 150 µm × 150 µm in a 300 µm thick silicon detector has a typical capacitance of 200...300 fF [Atl 97], compared to 8 fF from equation 3.2.

- The leakage current of the detector produces shot noise. To minimise its contribution, an optimal shaping time can be determined, if the leakage current is known. The leakage current of a 300 µm thick silicon detector is as low as 100 nA/cm^2. This scales down to 23 pA/(150 µm)^2 or 40 pA/(200 µm)^2. [Atl 97]

Bonding

To access a chip, connections to the pads must be made. In ordinary chips a chip core is surrounded by pads[10]. The complete chip is glued into a chip carrier by an electrically and thermally conducting solder paste. Connections are made by a wedge bonder via wire bonds. Small aluminium[11] wires (a diameter of 17 µm is often used) connect the pads with the chip carrier.

To connect a pixel detector to the dedicated electronic chip, a more sophisticated technique is used: The so-called bump bonding uses small beads to connect corresponding pads. On a wafer level an under bump metallisation (gold/nickel[12]) is formed on the electronic chip to allow enough adhesion to the aluminium pad. Through a mask a tin-lead solder is evaporated on the under bump metal. Afterwards

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[10] A typical pad is (100 µm)^2, the passivation opening is (85 µm)^2; a lateral pitch of 110 µm is achieved

[11] Strictly speaking: aluminium-silver alloy (with 1 % silver for better conductivity); gold wires are also used

[12] Beside gold and nickel also chrome, copper and titanium-tungsten are often used.

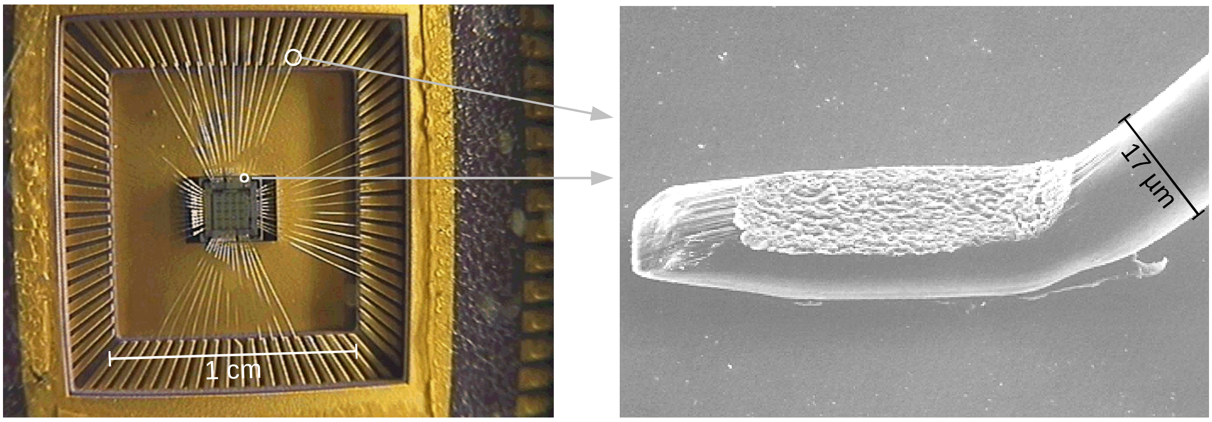

Figure 3.4 Wire bonding: Chip in carrier (Ramses 1) and a magnified view of a wedge bond

a solder ball is formed by reflow. The detector is headlong (flip chip) roughly aligned[13] on the electronic chip. A reheat melts the bump balls and solders both components together. The surface tension cares for a precise alignment. A bump bond pad pitch[14] lower than 50 µm can be handled.

The handling of a single chip is considerably harder. Either a dummy wafer must be used, in which the chip is integrated to undergo the previously mentioned process, or a different technique is chosen: Each single bump is placed by an adapted wire bond machine. Figure 3.5 shows the idea of bump bonding and a magnified view of a single gold stud bond.

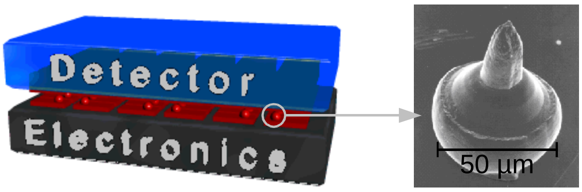

Figure 3.5 Bump bonding: Connection between detector and electronic chip; magnified view of a gold stud bond

An overview of various bonding techniques is given by [Npg 01].

3.3.6 Summary of Properties of Selected Semiconductors

The chapter is closed by summarising the main properties of some important semiconductors, which are given in Table 3.1 [Sze 81], [Lut 99], [Wan 89].

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[13] The footprint of the electronic chip and the detector have to match of course.

[14] A diameter of the passivation opening of 12 µm on a 18 µm pad is used in ATLAS [Atl 97].

substance	Silicon (Si)	Germanium (Ge)	Gallium-Arsenide (GaAs)	Diamond (C)
atomic number	14	32	31...33	6
average atomic mass	28.09	72.59	72.32	12.01
density [g/cm^3]	2.329	5.323	5.317	3.515
dielectric constant	11.9	16.2	12.9	5.7
melting point [°C]	1392...1415	917...937	1220...1238	3907
radiation length [cm]	9.36	2.30	2.3	12.15
lattice spacing [Å]	5.4307	5.657	5.653	3.5668
optical transition	indirect	indirect	direct	indirect
bandgap [eV] @ 300 K	1.12	0.66	1.42	5.47
mean energy for electron-hole pair generation [eV]	3.63	2.96	4.35	13.1
electron mobility [cm^2/Vs] @ 300 K	1450...1500	3900	8500...8800	1800
hole mobility [cm^2/Vs] @ 300 K	450...505	1800...1900	320...400	1200...1600
Fano factor F	0.115	0.13	0.10	0.08

Table 3.1 Properties of selected semiconductors

4 Readout Electronics

In contrast to HEP-experiments, where pixel detectors are used to track high energetic charged particles, which can be done by a fast digital readout, the requirements in a Compton camera are different. The attention is turned to a low noise readout, which is inconsistent with a fast readout. Also the analog information of the deposited energy is essential for the reconstruction. HEP-pixel detectors are mostly triggered externally – the Compton detector must be capable of self-triggering.

Due to the subtle segmentation of a pixel detector and the large number of readout channels, a low occupancy is achieved, i.e. most of the pixels are not hit by a single particle and contain no information. A sparse readout can therefore perform a significant data reduction (see section 4.12).

A dedicated ASIC (application specific integrated circuit), named RAMSES ("Rauscharme Analoge Pixel-Matrix-Signalverarbeitungselektronik aus Siegen": low noise analog pixel matrix readout from Siegen), for a Compton camera based on pixel detectors has been developed.

In this section the readout circuit as shown in Figure 4.1 will be presented: The positive charge generated in the detector or by an electrical test circuit is integrated by the charge sensitive amplifier (CSA). The ideal output signal of the CSA is a negative voltage step, which is split to a discriminator and a semi-gaussian shaper. As no external triggering information is available, the electronic has to be self-triggering, which is realised by the discriminator: A flag signalises if a given threshold is exceeded. Meanwhile the voltage step of the CSA is processed in a CRRC-shaper into an semi-gaussian shape. In the frequency domain the shaper limits the bandwidth of the signal to suppress thermal noise. In the time domain the maximum of the semi-gaussian pulse, which corresponds to the deposited energy, can simply be determined. The detection and storage of the maximum is realised in the peak detector, which is enabled and reset by the control logic. A subsequent unity gain buffer drives the large bus capacitance for readout of the analog value. The pixel control logic controls a timing circuit, which measures the time between a hit and the readout to permit an off-line reconstruction of the absolute trigger time. The absolute time information is necessary to associate corresponding hits of several detector planes, e. g. a coincidence of a Compton scattering and a photo effect.

The following sections will give a detailed discussion of each single block.

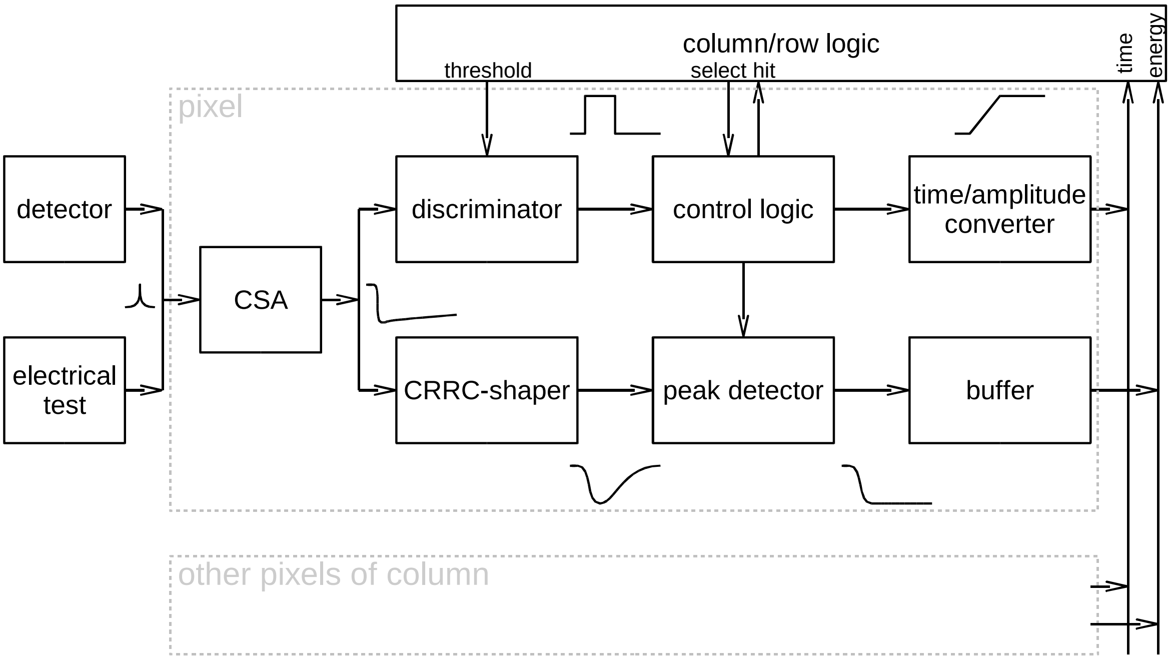

Figure 4.1 A block diagram of a pixel

To estimate the mean rate in a pixel, the following assumptions were made:

- A typical applied activity of radioactive Iodine to a patient is about 50 MBq
- The detector arrangement is about $r=2$ cm close to the organ under investigation, e. g. the thyroid gland
- The pixel size is 150×150 μm^2

The mean γ-quanta rate through a pixel is given by

$$\nu = 50\,\mathrm{MBq}\,\frac{(150\,\mu\mathrm{m})^2}{4\,\pi\,(2\,\mathrm{cm})^2} = 220\,\mathrm{Hz} \tag{4.1}$$

As the total interaction probability[15] of 30 keV γ-quanta in 300 µm thick silicon is about 0.1 [Ove 98], the mean rate of hits would be about 20 Hz.

4.1 Noise Considerations

To determine the noise contribution of a semiconductor detector readout electronic, the equivalent noise charge *(ENC)* is introduced: The noise measured at the system output is translated to an equivalent input charge, which would create the same signal size. The noise contributions can be subdivided into three types: thermal noise (ENC_d), flicker noise (ENC_f), shot noise (ENC_o). Their origins and contributions will be discussed in detail in the following subsections. As the noise sources are stochastically independent, the total *ENC* can be calculated according to

$$ENC_t^2 = ENC_d^2 + ENC_f^2 + ENC_o^2 \tag{4.2}$$

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[15] The interaction probability for 30 keV γ's in 300 µm silicon is dominated by photo effect. The corresponding interaction probability for Compton effect is about 0.01.

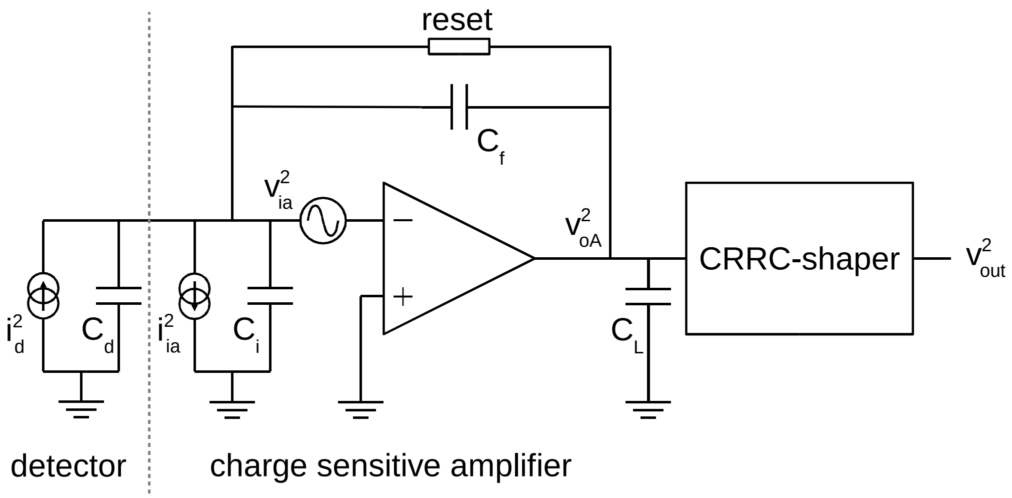

Figure 4.2 Noise model of the detector readout system

To calculate the equivalent input charge, a noise model shown in Figure 4.2 is used where v_{ia}^2 and i_{ia}^2 represent the equivalent input voltage and current noise generators of the electronic and i_d^2 represents the noise current associated with the detector leakage current I_0 and its bias network:

$$i_d^2 = 2qI_o + \frac{4kT}{R_B} \approx 2qI_o \tag{4.3}$$

The latter approximation is valid for a high value of the bias resistor R_B, e. g. for $I_0 \approx 100$ nA the second addend contributes less than 10 % at room temperature, if $R_B > 5$ MΩ. It should be noted that if the reset of the CSA is realised by means of resistive feedback, the noise current associated with the feedback resistance can be directly added to i_d^2.

The total noise power spectrum at the output of the CSA is given by [San 90]:

$$v_{oA}^2(i\omega) = \left|\frac{C_d + C_i + C_f}{C_f}\right|^2 v_{ia}^2 + \left|\frac{1}{i\omega C_f}\right|^2 i_d^2 \tag{4.4}$$

The detector capacitance and parasitic capacitances (e. g. due to connections) are subsumed in C_d. The effective input capacitance of the amplifier is labelled with C_i. C_f specifies the feedback capacitance. The equivalent electronic contribution v_{ia}^2 will be derived in section 4.2. To calculate the total output noise, the transfer function

$$H(s) = \left[\frac{s\tau_0}{1+s\tau_0}\right]\left[\frac{A}{1+s\tau_0}\right]^n \tag{4.5}$$

of a CRRC-shaper will be derived in section 4.3. Thus the total noise power of the CRRC-shaper is given by:

$$v_{tot}^2 = \int_0^\infty |v_{oA}(i\omega)|^2 |H(i\omega)|^2 df \quad \text{with} \quad \omega = 2\pi f \tag{4.6}$$

As will be shown in in section 4.3, the output signal of the shaper due to one electron generated in the detector is given by:

$$V_{outp}=\frac{q\,A^{n}\,n^{n}}{C_{f}\,n!\,e^{n}} \tag{4.7}$$

Herein the number n of integrators in the shaper and its amplification A must be known. Now the integral in equation 4.6 will be calculated for each noise component separately.

4.1.1 Thermal Noise

From equation 8.58 the equivalent thermal input noise associated with the channel resistance of the input MOSFET is given by

$$v_{ia}^{2}=\frac{8}{3}k\,T\frac{1}{g_{m}} \tag{4.8}$$

Using the equations 4.4 and 4.6 leads to

$$v_{totd}^{2}=\int_{0}^{\infty}\frac{8}{3}k\,T\frac{1}{g_{m}}\left(\frac{C_{t}}{C_{f}}\right)^{2}\frac{(\omega\tau_{o})^{2}A^{2n}}{\left(1+(\omega\tau_{o})^{2}\right)^{n+1}}df \tag{4.9}$$

where the total capacitance at the input node is $C_t=C_d+C_i+C_f$. The above integral can be solved in a closed form for all practical cases, where n is an integer:

$$v_{totd}^{2}=\frac{8}{3}k\,T\frac{1}{g_{m}}\left(\frac{C_{t}}{C_{f}}\right)^{2}\frac{A^{2n}g(n)}{4\pi\tau_{s}} \tag{4.10}$$

$$g(n):=n\cdot B(1.5,n-0.5)$$

$$B(z,w):=\int_{0}^{1}t^{z-1}(1-t)^{w-1}dt$$

B is the Euler Beta-function. The peaking time τ_s depends on the time constant τ_o of each integrating stage: $\tau_s=n\cdot\tau_o$. Dividing v_{totd} by the signal amplitude due to one electron charge (4.7), the equivalent noise charge ENC_d due to channel thermal noise is obtained:

$$ENC_{d}^{2}=\frac{8}{3}k\,T\frac{1}{g_{m}}\frac{C_{t}^{2}g(n)}{q^{2}4\pi\tau_{s}}\left(\frac{n!^{2}e^{2n}}{n^{2n}}\right) \tag{4.11}$$

For different n the values for *g(n)* and the last factor are given in the following table (4.1):

Considering equation 4.11 the following conclusions to reduce the thermal noise can be drawn:

n	1	2	3	4	5	coefficient for
$g(n)$	1.57	0.785	0.589	0.491	0.430	
$h(n)$	1.57	0.589	0.327	0.215	0.155	
$n!^2\,e^{2n}/n^{2n}$	7.39	13.65	19.92	26.20	32.48	
$\frac{n!^2\,e^{2n}/n^{2n}}{n}$	7.39	6.82	6.64	6.55	6.50	flicker noise
$g(n)\cdot(n!^2\,e^{2n}/n^{2n})$	11.61	10.72	11.74	12.86	13.95	thermal noise
$h(n)\cdot(n!^2\,e^{2n}/n^{2n})$	11.61	8.04	6.52	5.63	5.02	shot noise

Table 4.1 Factors depending on the order n

The CSA must be designed to have a transconductance g_m as large as possible while the total input capacitance must be minimised. Large peaking times τ_s reduce the thermal noise contribution. Finally the noise is independent of the gain of the shaper as both signal and noise are amplified by the same factor.

As both the total capacitance C_t and the transconductance g_m depend on the width of the input transistor, an optimal input width, which minimises the equivalent thermal input noise ENC_d, is found by taking the derivative of equation 4.11 with respect to W. The capacitance C_t depends linear on W:

$$C_t = C_0 + C_W \cdot W \tag{4.12}$$

Therefore the optimal input width can be calculated:

$$\frac{\partial ENC_d^2}{\partial W} \overset{!}{=} 0 = \frac{\partial}{\partial W}\left(\frac{(C_0 + C_W \cdot W)^2}{\sqrt{W}}\right) \Leftrightarrow C_W \cdot W = C_0 + C_W \cdot W \Leftrightarrow W_{opt} = \frac{C_0}{3\,C_W} \tag{4.13}$$

4.1.2 Flicker Noise

In the same manner the equivalent noise charge due to *1/f* noise will be calculated. The equivalent noise power v_{ia} due to flicker noise is given by

$$v_{ia}^2 = \frac{K_f}{C_{ox}^2\,W\,L\,f} \tag{4.14}$$

with the flicker noise coefficient K_f, the width W and length L of the input transistor, the gate oxide capacitance per unit area C_{ox} and the frequency f. Calculating equation 4.6 for the flicker noise power v_{ia} yields:

$$v_{totf}^2 = \int_0^\infty \frac{K_f}{C_{ox}^2\,W\,L\,f}\left(\frac{C_t}{C_f}\right)^2 \frac{(\omega\,\tau_o)^2 A^{2n}}{\left(1+(\omega\,\tau_o)^2\right)^{n+1}}\,df = \frac{K_f}{C_{ox}^2\,W\,L}\left(\frac{C_t}{C_f}\right)^2 \frac{A^{2n}}{2\,n} \tag{4.15}$$

The equivalent noise charge ENC_f due to flicker noise results in:

$$ENC_f^2 = \frac{K_f}{C_{ox}^2\,W\,L}\,\frac{C_t^2}{q^2\,2\,n}\left(\frac{n!^2\,e^{2n}}{n^{2n}}\right) \tag{4.16}$$

If flicker noise contributes significantly to the total noise, a PMOS transistor should be used, as it has a smaller flicker noise coefficient K_f than an NMOSFET.

The flicker noise coefficients[16] of the AMS[17]-0.6 µm-process are listed in table 4.2.

K_f(PMOS)	$0.54\cdot10^{-28}\ \mathrm{C^2/m^2}$
K_f(NMOS)	$15.4\cdot10^{-28}\ \mathrm{C^2/m^2}$

Table 4.2 Equivalent flicker noise coefficient K_f for PMOS and NMOS

Both the thermal noise and the flicker noise increase with the total capacitance. As the detector capacitance contributes a large portion to the total capacitance, the lower detector capacitance of pixel detectors compared to strip detectors results in a lower noise.

An analog calculation for the optimal width as for the thermal noise gives:

$$\frac{\partial ENC_f^2}{\partial W}\overset{!}{=}0=\frac{\partial}{\partial W}\left(\frac{(C_0+C_W\cdot W)^2}{W}\right)\Leftrightarrow 2\,C_W\cdot W=C_0+C_W\cdot W\Leftrightarrow W_{opt}=\frac{C_0}{C_W} \tag{4.17}$$

The optimal width to minimise the flicker noise contradicts the optimal width to minimise the thermal noise. To minimise the total noise, the optimal width between the to optima has to be found. As a rule of thumb, one can approximate the optimal gate width simply as the harmonic average[18] of both optima [Cha 97]. The flicker noise is almost independent of the number of integrators (see Table 4.1).

4.1.3 Shot Noise

Using the equivalent noise power i_d^2 given in equation 4.3, the noise component due to the detector leakage current I_o is calculated to be:

$$v_{toto}^2=\int_0^\infty \frac{2\,q\,I_o}{|i\,\omega\,C_f|^2}\frac{(\omega\,\tau_o)^2A^{2n}}{\left(1+(\omega\,\tau_o)^2\right)^{n+1}}\,df=2\,q\,I_o\frac{A^{2n}\tau_s h(n)}{C_f^2\,4\,\pi} \tag{4.18}$$

$$h(n):=\frac{1}{n}\cdot B(0.5,n+0.5)$$

Therefore the corresponding equivalent noise charge ENC_o due to shot noise is given by

$$ENC_o^2=2\,q\,I_o\frac{\tau_s h(n)}{q^2\,4\,\pi}\left(\frac{n!^2\,e^{2n}}{n^{2n}}\right) \tag{4.19}$$

The contribution of the shot noise to the total noise becomes smaller as the number of integrators increases (see Table 4.1).

---

[16] Equivalent flicker noise coefficients for I_{DS}=10 µA (regarding the respective flicker noise exponents *af*) are given.

[17] AMS: Austria Micro Systems

[18] The harmonic average *h* of two positive numbers *a*, *b* is given by *h=2ab/(a+b)*. The harmonic average is always smaller or equal than the geometrical and arithmetical average.

4.2 Charge Sensitive Amplifier (CSA)

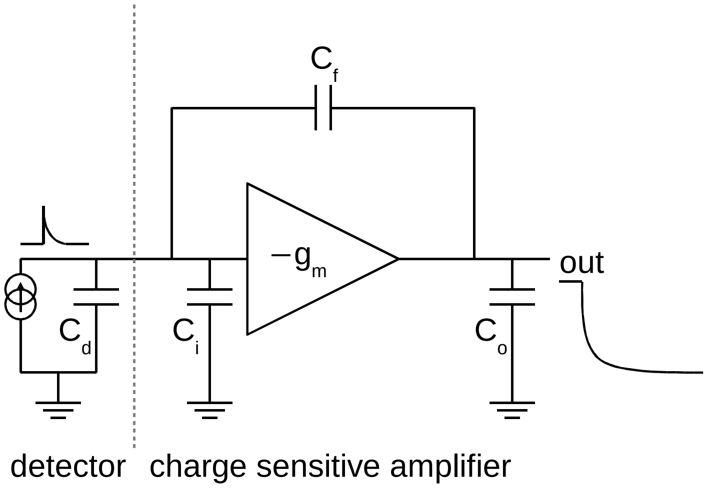

Figure 4.3 Simplified principle of operation of a charge sensitive amplifier (CSA)

The charge sensitive amplifier converts a charge generated in the detector to a voltage step by means of an inverting amplifier and a capacitive feedback. In Figure 4.3 a simplified diagram is sketched: The detector is drawn as a current source in parallel to the detector capacitance C_d. The charge sensitive amplifier consists of an inverting amplifier with the transconductance g_m and an equivalent input capacitance C_i. The capacitive feedback is referred to as C_f. The total output capacitance C_o summarises the load of the following stages as well as parasitic wiring capacitances.

An output voltage change dU_{out} causes an input voltage change dU_{in} through the feedback capacitor. The feedback factor $h_{fb}=dU_{in}/dU_{out}$ results from a capacitive voltage divider of C_f, C_d and C_i:

$$h_{fb}=\frac{C_f}{C_d+C_i+C_f} \tag{4.20}$$

The total load seen be the amplifier is the sum of the output capacitance of the preamplifier, the parasitic wiring capacitance to the next stage, the input capacitance of the next stage and the contribution of the feedback, which is a capacitive voltage divider of the feedback capacitor C_f on the one hand and the parallel connection of the detector capacitance C_d and equivalent input capacitance C_i on the other hand:

$$C_L=C_o+h_{fb}(C_d+C_i) \tag{4.21}$$

Solving

$$|dU_{out}|=|dI_{out}\cdot Z_{out}|=|dU_{in}\cdot g_m\cdot\frac{1}{i\,\omega\,C_L}| \tag{4.22}$$

for ω leads to the integrating time constant τ_a of the amplifier

$$\tau_a=\frac{1}{\omega}=\frac{C_L}{h_{fb}\,g_m} \tag{4.23}$$

A charge dQ_{in} deposited at the input produces a voltage input swing of $dU_{in}=dQ_{in}/C_{in}$. The input capacitance $C_{in}=C_d+C_i+(1+A_V)\cdot C_f$ with a voltage amplification denoted by $A_V=-dU_{out}/dU_{in}$. Solving for dU_{out} yields:

$$dU_{out}=\frac{-dQ_{in}}{C_f+\frac{C_d+C_i+C_f}{A_V}}\approx\frac{-dQ_{in}}{C_f} \tag{4.24}$$

For a sufficient large voltage amplification the charge from the detector is almost completely pumped on the feedback capacitance. The charge to voltage amplification is therefore given by:

$$A=\left|\frac{dU_{out}}{dQ_{in}}\right|=\frac{1}{C_f} \tag{4.25}$$

4.2.1 Input Noise Matching Conditions

The total noise performance of the entire system is by far dominated by the input transistor. In a reasonable design it contributes more than 95 % to the total output noise [Cha 97]. Therefore it is worthwhile to dedicate a whole subsection on the choice of this transistor.

The basic design parameters of the input transistor are its polarity, the geometry (width, length) and the DC-bias current. Together with the shaper peaking time τ_S and the order n of the shaper this forms a five dimensional optimisation problem, which will be solved iterative below.

The capacitance of the input transistor is given by the transistor width W, the length L and the oxide capacitance per unit area $C_{ox}=\varepsilon_{ox}/t_{ox}$. [Wes 94]:

$$C_{gs}=C_{gd}=\frac{\varepsilon_{ox}WL}{2t_{ox}}=\frac{1}{2}C_{ox}WL \tag{4.26}$$

Herein ε_{ox} denotes the dielectric constant of silicon dioxide and t_{ox} the oxide thickness. To maximise the signal to noise ratio, one claims for a high voltage gain in the first stage. As described in the appendix, a cascoded configuration will be chosen to reduce the input capacitance due to Miller effect. Depending on the input resistance of the cascode transistor $(1/g_m^{casc})$ the gate drain capacitance seems to be enlarged by a factor $(1+g_m^{input}/g_m^{casc})$. By using a regulated cascode the g_m^{casc} can be designed[19] to be as large as g_m^{input}. Assuming $g_m^{input}=g_m^{casc}$ and a minimum length transistor $(L=0.6\ \mu\text{m})$, the width-dependent capacitance C_W can be calculated:

$$C_W=\frac{C_{gs}+2C_{gd}}{W}=\frac{3}{2}C_{ox}L\approx 2.5\,\text{fF}/\mu\text{m} \tag{4.27}$$

Using equation 4.27, replacing W in g_m of (4.11) by W_{opt} of (4.13) and substituting C_t by 4.12 yields:

---

[19] As the input transistor will be biased with a higher current than the cascode transistor, it is hard to achieve the same g_m with a simple cascode configuration.

$$ENC_{dopt}^2 \propto \frac{C_t^2}{g_m} = \frac{(C_0 + W_{opt} \cdot C_W)^2}{\sqrt{2I \frac{W_{opt}}{L} KP}} = \frac{\left(\frac{4}{3} C_0\right)^2}{\sqrt{2I \frac{C_0}{3 C_W L} KP}} \propto \frac{C_0^{1.5}}{\sqrt{\frac{I}{L^2}}} = L \frac{C_0^{1.5}}{\sqrt{I}} \tag{4.28}$$

An analog derivation for (4.16) with (4.17) yields:

$$ENC_{fopt}^2 \propto \frac{K_f C_t^2}{W_{opt} L} = \frac{K_f (C_0 + W_{opt} \cdot C_W)^2}{\frac{C_0}{C_W} L} \propto \frac{K_f C_0}{\frac{L}{C_{ox} L}} \propto C_0 K_f \tag{4.29}$$

The total noise is therefore minimised by using

- capacitive input matching
- minimal gate length L (technology limit)
- high bias current I for large g_m (limited by power consumption)
- transistor with lowest flicker noise coefficient K_f, i. e. PMOS

4.2.2 Design Considerations

The CSA is going to be designed for a "p-in-n"-detector: The pixels consist of strongly doped p^+-implantation areas in a weakly doped n^--substrate. To achieve a large sensitive volume, the depletion zone is expanded by reverse biasing these junctions, wherefore the backside of the detector is connected to a positive high voltage source. The positive charges therefore migrate to the more negative p-contact, where they are collected by the CSA. The response of the CSA to positive charges is a negative output swing due to the inverting characteristic. To provide the maximal possible output swing, the DC-level of the CSA-output is held as high as possible (near the positive power supply). To achieve this and providing a low output resistance at the same time and a fast rise time for the leading edge (negative slope), a PMOS-source follower is used as the output stage.

Via the DC-feedback (see next section) the operating point of the input transistor is set to approximately the same voltage level as the output of the CSA. To set the highest possible DC-level, the source of the PMOS-input-FET, which is optimised for low noise, is directly connected to the positive analog power supply voltage V_{DDA}. The input stage and the output buffer are shown in Figure 4.4.

As described in the previous section, a regulated cascode configuration is used for two reasons:

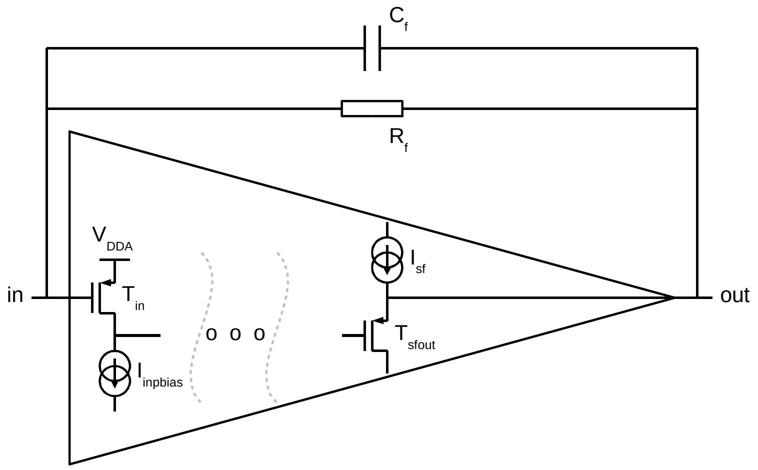

Figure 4.4 Detailed view of the input stage and the output buffer of the CSA

- lower the load resistance seen by the input transistor to keep the voltage gain low to minimise the influence of the parasitic gate-drain capacitor (large GBW ⇒ short rise time)
- provide a large current to voltage gain of the cascode stage to provide a large overall amplification

The complete schematic of the CSA is shown in Figure 4.5.

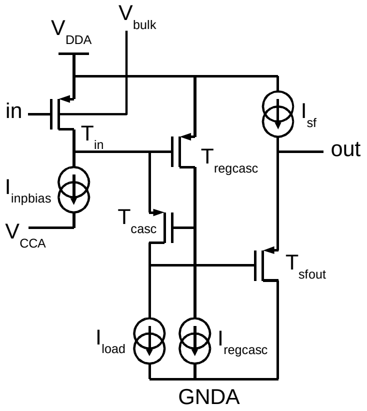

Figure 4.5 Complete amplifier design for the CSA

The relatively high input bias current $I_{inpbias}$ (large g_m, low noise) is sunk by an additional voltage V_{CCA} to reduce the voltage drop across the input bias current source and the input transistor to save power. In the implemented design all shown current sources are realised as current mirrors. The currents are globally set by DACs. To reduce the influence of the parasitic JFET (bulk potential controls the drain current) in the input transistor, the bulk contact can be pulled to a higher potential than V_{DDA}.

The range of the optimal input transistor width is calculated by substituting C_W from 4.27 in equation 4.13 and 4.17. Assuming a detector capacitance[20] of 350 fF and a parasitic capacitance (wires and bond-pad) of 100 fF, this yields:

$$\frac{C_0}{3C_W}=\frac{450\,\text{fF}}{3\cdot 2.5\,\text{fF}/\mu\text{m}}=60\,\mu\text{m}\leqslant W_{opt}\leqslant 180\,\mu\text{m}=\frac{C_0}{C_W} \tag{4.30}$$

The harmonic average of both optima leads to an optimal width of 90 µm. Due to design rule limitations an input transistor width of 107.2 µm is realised. Figure 4.6 shows the layout of the implemented input transistor. The input transistor consists of eight transistors (W=13.4 µm) in parallel to reduce the gate-resistance (33 $\Omega\cdot W/L/n$=737/8=92 Ω), because a single gate of W=107.2 µm would have a resistance of 5900 Ω (33 $\Omega\cdot 107.2/0.6$). By sharing both source and drain between two transistors, the effective capacitances (gate-drain and gate-source) are reduced.

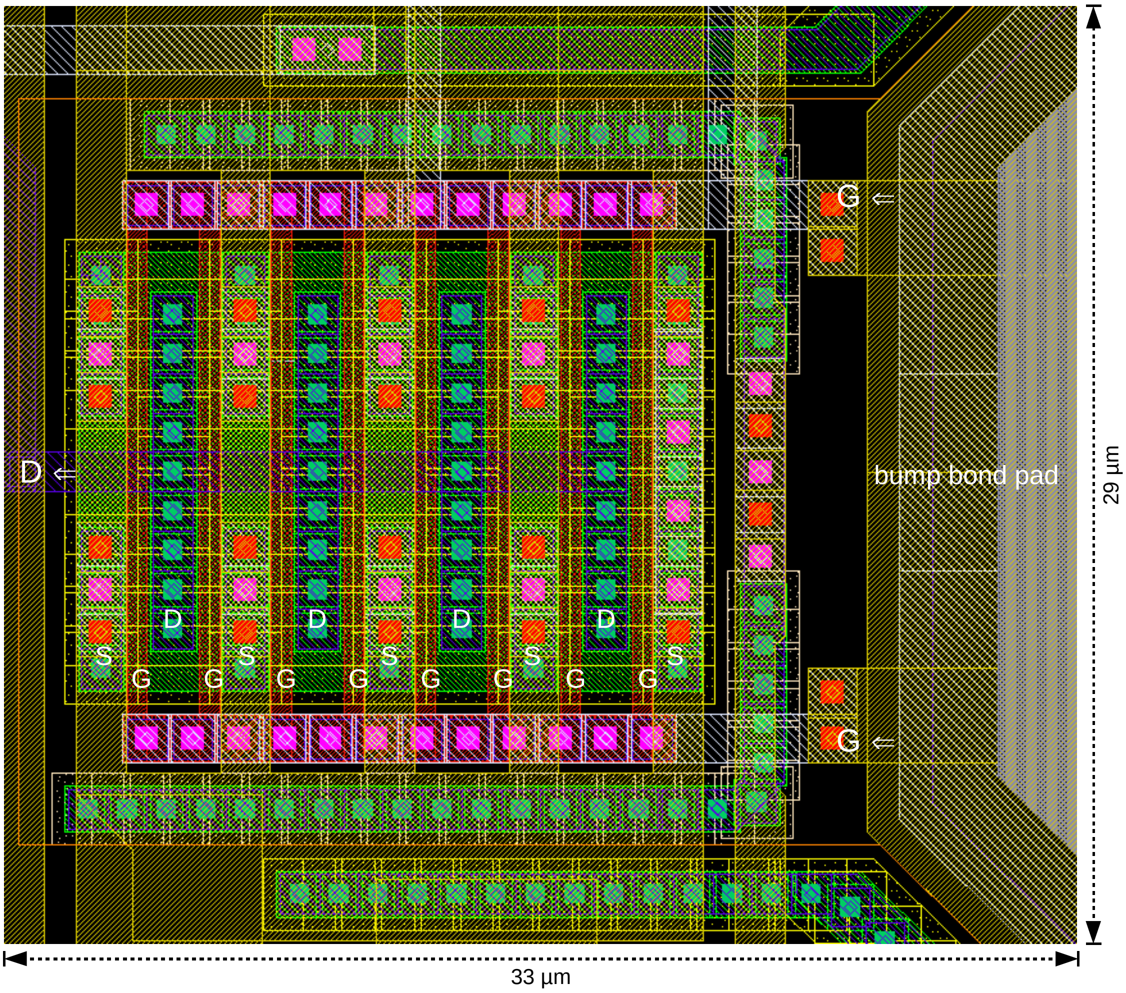

Figure 4.6 Implemented input transistor: Eight transistors with shared drains and sources form an effective input transistor with W/L=107.2/0.6

The required gain bandwidth product *(GBW)* depends on the attenuating factor $1/h_{fb}$ (see equation 4.20) and the rise time (t_r) requirements [Cha 97]:

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[20] A detector capacitance of 200 fF for a $(150\ \mu\text{m})^2$-pixel scaled to a $(200\ \mu\text{m})^2$-pixel

$$GBW = \frac{2.2}{2\pi h_{fb} t_r} \tag{4.31}$$

Assuming a total capacitance of 650 fF (additional input capacitance of 200 fF), a rise time of 200 ns (noticeable smaller than the peaking time in the order of µs) and an effective feedback capacitance of 0.5 fF yields a GBW of 2.3 GHz.

Using equation 4.23, the GBW can be written as:

$$GBW = \frac{dU_{out}}{dU_{in}} \nu_{-3dB} \approx \frac{g_m}{2\pi(C_o + C_f)} \tag{4.32}$$

The output stage of the amplifier forms a load capacitance of C_o=50 fF, requiring an input transistor transconductance of

$$g_m = 2\pi(C_o + C_f) GBW = \frac{2.2(C_o + C_f)}{h_{fb}\, t_r} = 0.7\,\mathrm{mS} \tag{4.33}$$

From equation 8.12 the bias current can be calculated:

$$I = \frac{g_m^2}{2KP} \frac{L}{W} \tag{4.34}$$

For the chosen width of 107.2 µm and a minimum length (L=0.6 µm) the bias current for a PMOS transistor must be 33 µA, which is a relatively large current, just within the power budget, explaining the additional supply voltage V_{CCA} to reduce the power consumption.

Having optimised the input transistor, the current mirrors have to be optimised for low noise. As will be shown in section 8.3.2 by using 1:1-mirrors and small W/L the noise contribution can be reduced. Smaller W/L needs higher $V_{GS} - V_{thr}$ for a required current, which is better for matching, but also a higher output voltage (V_{DS}) is required to keep the transistor in saturation. This reduces the possible output swing. A compromise between the required output swing and the noise contribution must be found.

The currents I_{load} and $I_{regcasc}$ are dimensioned to provide a low input resistance seen by the input transistor to achieve the low voltage gain in the input stage. To achieve a voltage gain $(g_m \cdot R_{load})$ significant lower than unity, the input resistance of the regulated cascode stage must be smaller than 1/0.7 mS=1.4 kΩ. With relatively small transistors (W/L=5 µm/0.6 µm) and a moderate current of I_{load}=2 µA an input resistance of 930 Ω can be realised (see section 8.3.3). In the design $I_{load} = 3 \cdot I_{regcasc}$ is realised by a fixed W/L-ratio.

The current of the source follower I_{sf} can be relatively low as well (typ. 1 µA) as the rise time of the leading edge (negative slope) is not limited by the DC-bias in contrast to the trailing edge.

With these design parameters, a total input capacitance of C_t=650 fF, a temperature of T=300 K, an input bias current of 30 µA, a shaping time of τ_s=1 µs and a subsequent first order shaper the noise contributions (equations 4.11, 4.16) are calculated:

$$ENC_d=\sqrt{2.46\frac{k\,T}{q}\,\frac{C_t^2}{q\,g_m\,\tau_s}}=\begin{matrix}16.0\text{e for PMOS}\\12.2\text{e for NMOS}\end{matrix} \tag{4.35}$$

$$ENC_f=\sqrt{3.7\frac{K_f}{C_{ox}^2\,W\,L}\,\frac{C_t^2}{q^2}}=\begin{matrix}4.0\text{e for PMOS}\\16.8\text{e for NMOS}\end{matrix}$$

For comparison the equivalent noise for an NMOS input transistor is given. The input referred noise $\sqrt{ENC_d^2+ENC_f^2}$ in the PMOS transistor is with 16.5 e about 30 % lower than the noise of 20.7 e of an NMOS.

4.2.3 Feedback Network

As shown in Figure 4.7 the feedback network usually consists of a capacitor *(C_f)* and a resistor *(R_f)*. The feedback capacitor accumulates the detector charge and converts it to a voltage *($\Delta Q_{det}=C_f\cdot\Delta U_{out}$)* whereas the feedback resistor is a reset mechanism.

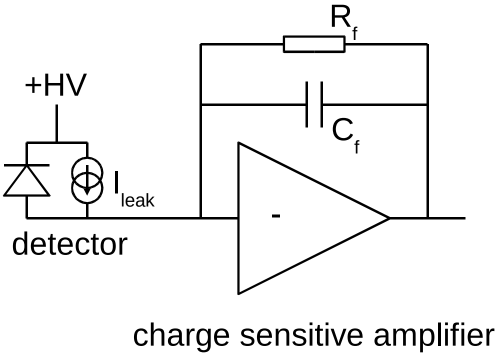

Figure 4.7 CSA with feedback resistor and capacitor

The implemented capacitor value can be determined by the maximal detector charge and output swing. In the primary application iodine 123 was designated to be used. Beside the 159 keV-γ-quant of I^{123}, which is already used in SPECT, it emits γ's of 27.4 keV (K_α). To have a small margin, the CSA should be designed for an γ-energy of 30 keV. Assuming a maximal γ-energy of 30 keV, which generates 8300 eh-pairs in silicon (3.6 eV/eh-pair), and that the maximal output swing is limited by less than the power supply (3 V nom.), the feedback capacitor has to be less than 0.5 fF, which is extremely small even for integrated circuits.

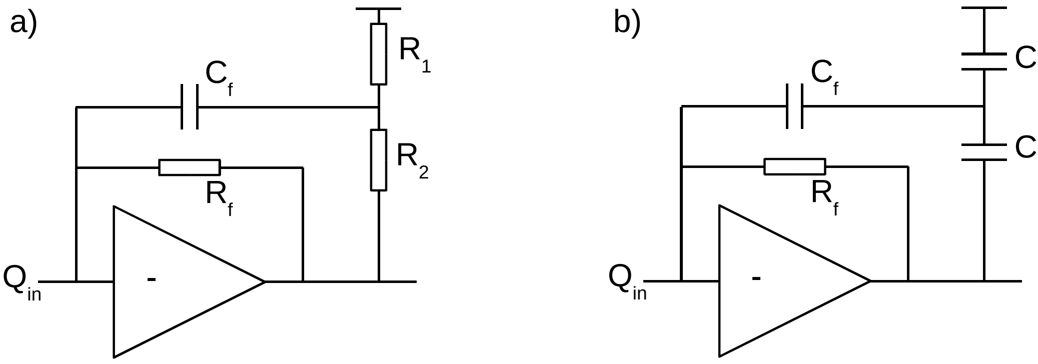

Figure 4.8 Two realisations of a voltage divider between output of CSA and feedback capacitor: a) resistive divider, b) capacitive divider

To obtain a large output swing for a given input charge, only part of the output step is fed to the feedback capacitor. Therefore the voltage across the feedback capacitor can be smaller than the output voltage, which allows a larger, but feasible, feedback capacitance. The smallest realisable accurate capacitor can be as small as 2 fF. A voltage divider of 1:4 must be realised. In Figure 4.8 two realisations of a voltage divider are shown: a resistive and a capacitive divider. For the resistive divider the voltage is divided by $R_1/(R_1+R_2)$. In the DC-condition the CSA has to drive the resistive load. From the power budget side the current can be some µA. As a consequence the resistors must be as large as MΩ, which is hard to achieve. Another possibility is a capacitive divider, which sinks no current at DC, but divides the voltage step as $Z_1/(Z_1+Z_2)=C_2/(C_1+C_2)$. As a constraint the capacitors C_1 and C_2 should be large compared to C_f. to achieve an accurate division.

In both cases a simple switch across R_2 or C_2 respectively, leaves the possibility of a range selection, which might be useful, if the same electronic chip is used for different detector layers: A small range but large voltage step per electron to detect Compton scattering and a large range but smaller voltage step per electron to detect a photo effect.

Beside the choice of the feedback capacitor, one has to pay attention to the feedback resistor, which has three tasks:

1. To sink the leakage current of the detector, as the amplifier input is a MOSFET-gate, unable to sink any current
2. Discharge the feedback capacitor to avoid pile up
3. Set the DC operating point of the amplifier input through a high resistive connection to the output

On the one hand from the requirement of low noise the thermal noise contribution of the feedback resistor should be kept lower than the noise contribution of the detector leakage current:

$$i_f^2 = \frac{4kT}{R_f} \ll 2qI_o = i_d^2 \qquad (4.36)$$
$$\Leftrightarrow R_f \gg 2\frac{kT}{q}\frac{1}{I_o}$$

On the other hand the leakage current flowing through the feedback resistor causes a voltage drop between input and output of the CSA reducing the maximal output swing and thus the energy range. The maximal signal rate $(\sim 1/\tau_f = 1/(R_f C_f))$ of the detector is also limited by the time constant of the feedback network. As will be shown in the subsection of the CRRC-shaper, for best signal to noise ratio the time constant of the feedback network has to be significantly larger than the shaper's time constant.

The leakage current of a (200 µm)^2 pixel is typically 40 pA (see section 3.3.4). According to equation 4.36 a reasonable feedback resistor has a value much larger than 1 GΩ at room temperature, which can only be achieved by a transistor operated in weak inversion. As the leakage current varies from pixel to pixel and with temperature and as the process parameters of transistors have a dispersion, the bias voltage of this feedback transistor has to be generated for each pixel individually. In the second version of the readout electronics a two bit digital-/analog converter was realised in each pixel, which individually slightly modified the global bias voltage. Since the variation over all pixels was larger than expected, an auto-adaptive method as suggested by Krummenacher [Kru 91] has been used in a third version. Assuming no feedback resistance, the leakage current slowly charges the input capacitance of the CSA as illustrated in Figure 4.9. As soon as the DC-operating point is reached, the output of the CSA rapidly changes due to the large voltage amplification of the configuration. Krummenacher's idea is to sink exactly the leakage current by holding the input at the DC-operating point. The regulation of the leakage current sink is managed by monitoring the CSA output voltage and comparing it to a reference voltage.

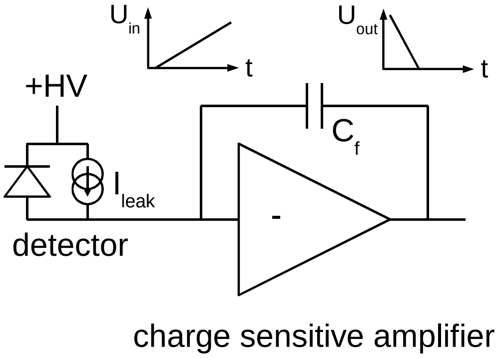

Figure 4.9 Without any feedback resistance the input capacitance is charged by the leakage current

The suggestion of Krummenacher needs a reference current in the order of 10 pA, which is hard to achieve. Therefore a modification of the circuit is realised: A transistor in weak inversion sinks the leakage current of the detector as shown in Figure 4.10.

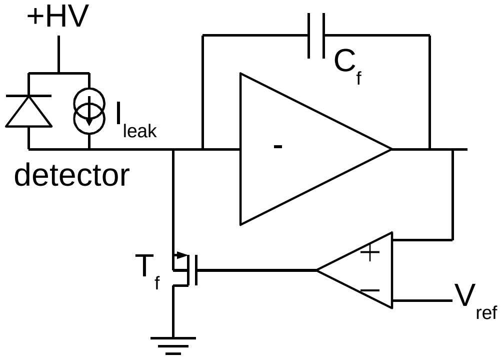

Figure 4.10 Monitoring the CSA-output to determine, if the leakage current is compensated

The presented circuit exactly sinks the leakage current. (Assuming the leakage current would exceed the current sunk by T_f, the input of the CSA would be pulled high. The inverting output of the CSA drops below the reference voltage V_{ref}, causing T_f to be readjusted to sink a higher current.)

To avoid that a detector signal charge is sunk directly by T_f, the mean output voltage of the CSA is compared with the reference voltage, which presumes a relative slowly (compared to a signal) changing leakage current. The mean output voltage is determined by an RC-filter or a C/g_m-filter respectively, as shown in Figure 4.11.

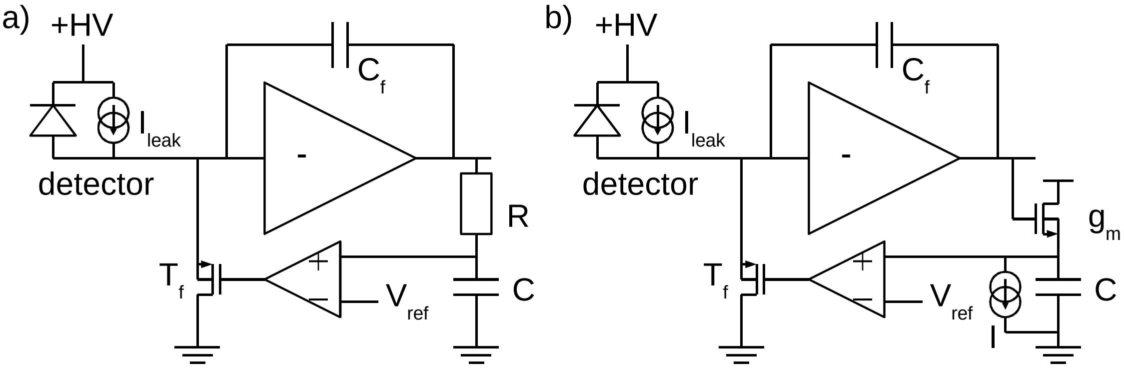

Figure 4.11 Averaging of output voltage by a) RC-filter or b) C/g_m-filter

The feedback resistance is now completely substituted by T_f. The effective resistance $R=dU_{in}/dI_{in}=dV_{GS}/dI_{in}=1/g_m$. As shown in 8.1.1 the transconductance in subthreshold is given by

$$g_m \approx \frac{q}{n\,k\,T} I_{leak} \tag{4.37}$$

So the effective resistance decreases with increasing leakage current.

The noise contribution of this feedback can be directly added to i_d^2 in equation 4.3:

$$i_d^2 = 2\,q\,I_{leak} + \frac{8\,k\,T\,g_m}{3} = 2\,q\,I_{leak}\left(1 + \frac{4}{3\,n}\right) \tag{4.38}$$

For n=1.33 the noise contribution of the feedback is as high as the leakage current noise. To calculate the overall noise, the double leakage current can simply be used.

A complete layout of the CSA is shown in Figure 4.12.

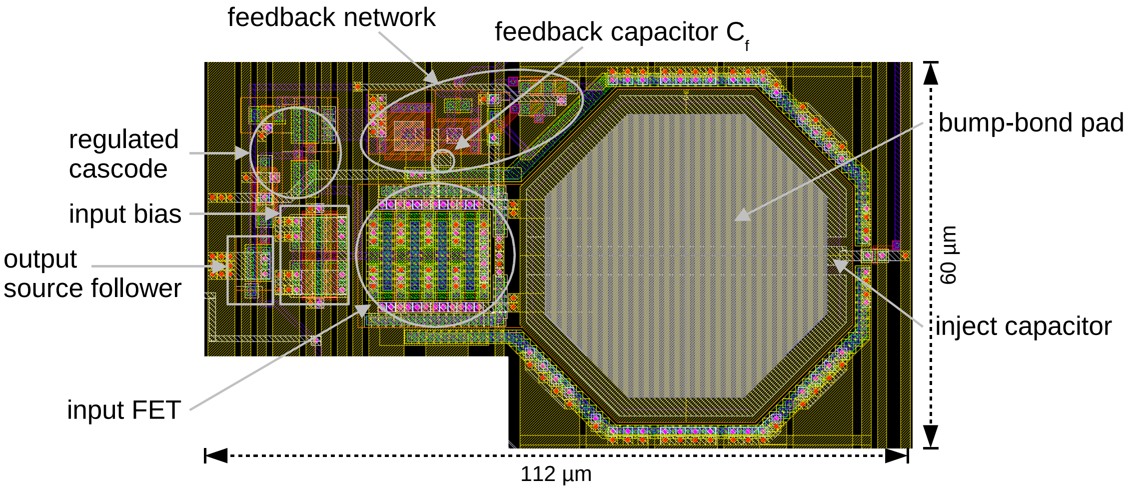

Figure 4.12 Layout of the charge sensitive amplifier (CSA)

The corresponding schematic is shown in Figure 4.13.

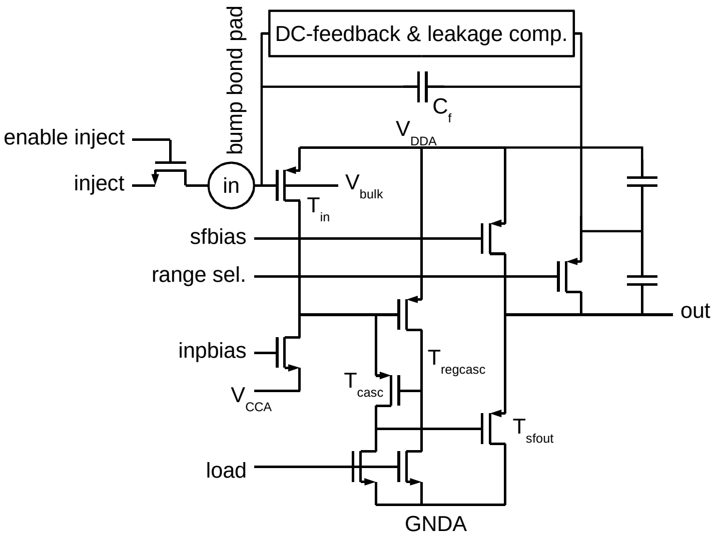

Figure 4.13 Complete schematic of the CSA

4.3 CRRC-Shaper

The shaper has two tasks: To trim the frequency range to reduce thermal noise (frequency domain) and to transform the size of the step response of the CSA to a semi-gaussian pulse (S-G), whose maximum can easily be measured (time domain).

From the noise point of view the ideal shaper transfer function (cusp-function) is derived in [Rad 88]. There are two drawback of the ideal transfer function: The signal response in the time domain is very cuspid, which makes it difficult to detect and store. Another drawback is the circuit complexity, which cannot be managed in each pixel, where the area for electronics is strongly limited. Popular shapers are based on several resistor-capacitance filters (RC) and one or two differentiation stages (CR).

To get rid of possible DC-offsets at the CSA-output, a differentiating CR-stage is couple to the CSA-output. To detect the height of the maximum of the peak, the integral, which is proportional to the maximum, is measured by means of a subsequent RC-integrator.

In the frequency domain the CR-RC-chain forms a bandpass, which suppresses low and high frequencies. This improves the signal to noise ratio (S/N), assuming white noise.

The transfer function of a CR-RC shaper is the product of the transfer function of a high-pass filter and a low-pass filter, which result simply from the voltage divider, built of a capacitor and resistor:

$$H(s)=\left[\frac{s\tau_0}{1+s\tau_0}\right]\left[\frac{A}{1+s\tau_0}\right]^n \tag{4.39}$$

The optimal S/N is achieved, if both the time constants of the differentiator and of the integrator are equal [Gat 86].

To calculate the pulse signal in the time domain, it is reasonable to approximate the output of the CSA as an ideal step with an amplitude of Q/C_f, as the rise time of the step signal at the output of the CSA is normally much shorter than the peaking time of the shaper. In this case, the output signal in the frequency domain is given by

$$V_{out}(s)=\left[\frac{s\tau_0}{1+s\tau_0}\right]\left[\frac{A}{1+s\tau_0}\right]^n\frac{Q}{sC_f} \tag{4.40}$$

where $Q/(sC_f)$ is the Laplace transform of an idealised step signal. By taking the inverse Laplace transformation of equation 4.40, the output signal in the time domain is obtained:

$$V_{out}(t)=\frac{QA^n n^n}{C_f n!}\left(\frac{t}{\tau_s}\right)^n e^{-nt/\tau_s} \tag{4.41}$$

The peaking time (V_{out} reaches maximum) of the shaper τ_s is defined by $\tau_s=n\tau_0$. The peak amplitude of the CRRC-shaper is calculated by evaluating (4.41) at the peaking time τ_s:

$$V_{out}(\tau_s)=\frac{QA^n n^n}{C_f n!\, e^n} \tag{4.42}$$

The normalised output voltage for different number of integrating elements are shown in Figure 4.14.

For a higher counting rate, a larger number of integrators is used to achieve a relatively fast return to baseline. From the noise point of view, if thermal noise is

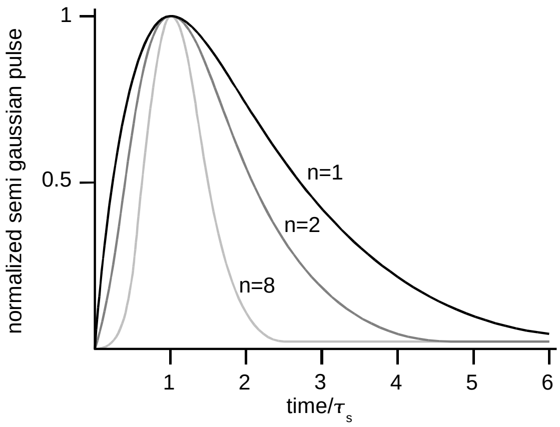

Figure 4.14 Normalised output signal of semi gaussian shapers with n integrating elements

dominant, then a second order shaper is ideal (see Table 4.1). On the other hand the area in a pixel is limited, so the quantity of elements used in each pixel must be kept low. As will be shown below, capacitors need a relatively large area. As a consequence a first order shaper has been implemented.

Two practical realisations of a CRRC shaper are shown in Figure 4.15. The first solution (a) is self-evident: A differentiation element (CR) is followed by an integrator (RC). An additional unity gain buffer between both stages reduces the load of the first stage. The second solution (b) shows an inverting realisation, which uses the current signal of the first stage (CR) flowing into a parallel CR element. The frequency behaviour of this arrangement is exactly the same as in (a), but in the time domain the output signal is inverted. In CMOS an arrangement, in which a voltage is converted to a current and vice versa is used, because the MOSFET itself is an device converting an input voltage to an output current.

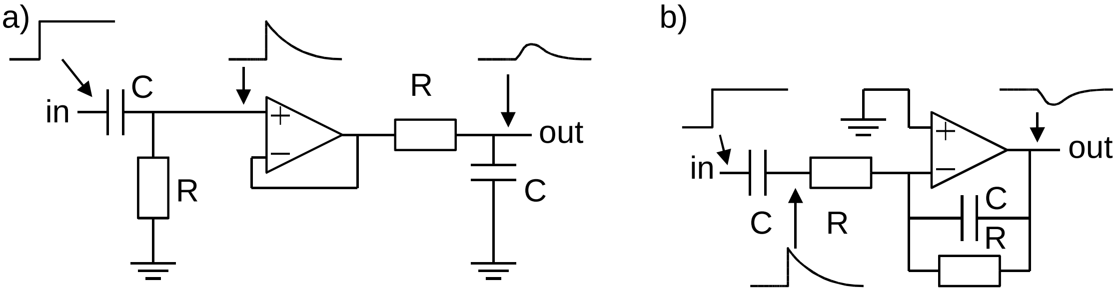

Figure 4.15 CR-RC shaper: a) A straight forward solution b) An inverting realisation

Depending on the detector leakage current it turns out that the optimal peaking time of the shaper is in the microsecond range *(τ=RC)*. In the given technology a capacitor of 500 fF occupies approximately 800 µm^2, which is 1/12 of the area of a 100×100 µm pixel. Hence the resistor has to be in the order of several MΩ. A standard polysilicon resistor of that size is impractical to place in a pixel. Moreover the shaping time would be fixed for a given resistor and a given capacitor, which is mostly undesirable. An adjustable solution is sought to realise the optimal shaping time. The resistor is replaced by a long diode connected transistor. A diode connected transistor has a small signal impedance of $1/g_m$. As shown in equation 8.12 the transconductance g_m depends on the current I, the transistor dimensions (width W, length L) and the transconductance parameter KP:

$$g_m \approx \sqrt{2 \frac{W}{L} KP\, I} \tag{4.43}$$

For a large resistance (small g_m) a low DC current, a narrow and long transistor and a PMOS (lower KP) should be used.

The implemented shaper is shown in Figure 4.16: T_1 and T_5 act as resistances and have the same dimensions. The current I sets the operating point and therefore the g_m of T_1. As the current is mirrored via the two current mirror T_1, T_2 and T_3, T_4, the g_m of T_5 is exactly set to the same value. Applying a (negative) voltage step on the input, the capacitor C and the resistance of T_1 form a differentiator. For small signals the current through T_1 changes proportional to the voltage across T_1. This current change is mirrored by $T_{1,2}$ and $T_{3,4}$ and applied on T_5 || C, where it is integrated and producing the desired output voltage shape.

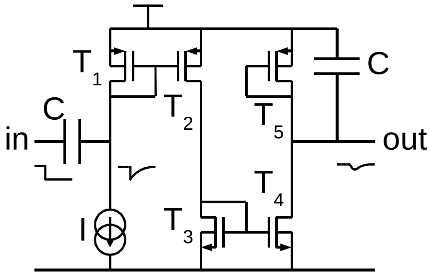

Figure 4.16 Shaper implementation

If the shaper has no intrinsic amplification, the output voltage peak is $1/e$ of the input voltage step (see equation 4.42). To introduce an additional amplification, the current change in T_1 due to a signal has to be amplified. This can be done by an appropriate ratio in the current mirror $T_{3,4}$. On the other hand, the DC current through T_5 must be the same as through T_1 to retain the same g_m, which can be achieved by bypassing an adequate current along T_5. The final solution is shown in Figure 4.17: The current is multiplied by $T_{3,4}$ with a factor m. Subtracting the $(m-1)$-fold of I yields to a DC current I through T_5. Applying an additional current signal dI on T_1 yields to an additional current signal into C || T_5 of $m \cdot dI$, which results in a m times larger output voltage.

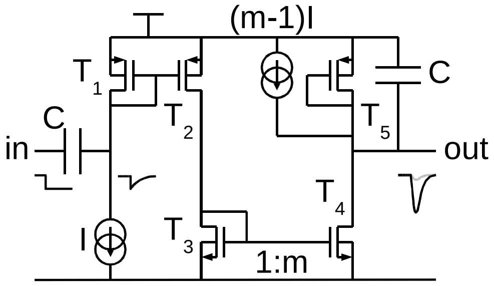

Figure 4.17 Shaper implementation with integrated amplification

By adjusting the current I, the effective resistance of T_1 and T_5 are modified in the same way resulting in a different shaping time. A drawback of the presented circuit is the change in g_m for large signals (non optimal shaping time), which can be accepted, because in the considered application only the small signals (Compton signals) need to be detected with low noise.

To determine the optimal shaping time for low noise, the thermal noise has to be compared to the shot noise: On the one hand a longer shaping time corresponds to a lower bandwidth, which reduces the white thermal noise. On the other hand the detector leakage current fluctuations are summed up for a longer time: The optimal shaping time, where the shot noise competes with the thermal noise, can be found.

Both noise contributions are repeated for a first order shaper:

$$ENC_d=\sqrt{2.46\frac{k\,T}{q}\,\frac{C_t^2}{q\,g_m\,\tau_s}} \tag{4.44}$$

$$ENC_o=\sqrt{1.85\frac{I_o}{q}\tau_s}$$

The optimum shaping time can be calculated by taking the derivative of $ENC_d^2+ENC_o^2$ with respect to τ_s or from the condition that $ENC_d=ENC_o$:

$$0=\frac{\partial}{\partial\tau_s}\left(ENC_d^2+ENC_o^2\right)=-2.46\frac{k\,T}{q}\,\frac{C_t^2}{q\,g_m\,\tau_s^2}+1.85\frac{I_o}{q} \tag{4.45}$$

Solving for τ_s yields:

$$\tau_s=C_t\sqrt{\frac{k\,T}{q}\,\frac{4}{3\,I_o\,g_m}} \tag{4.46}$$

For C_t=650 fF, T=300 K, I_0=10 pA, g_m=0.7 mS the optimal shaping time amounts τ_s=1.44 µs.

Calculating the total input referred noise yields (without feedback contribution):

$$ENC_t=\sqrt{ENC_d^2+ENC_f^2+ENC_o^2}=\sqrt{(12.9\,e)^2+(4.0\,e)^2+(12.9\,e)^2}=18.7\,e \tag{4.47}$$

For a leakage current of I_0=40 pA for a (200 µm)^2-pixel (expected from the detector specifications 100 nA/cm^2) and considering the noise of the feedback transistor, an optimal shaping time of 500 ns is calculated for a total expected noise of ENC_t=31 e.

4.4 Discriminator

Each pixel must be able to determine an interesting event, when an incident γ-ray deposits energy in the detector, causing a step response of the CSA. As no external triggering signal is available, the output of the CSA has to be observed. If the output suddenly changes more than a certain amount, a valid hit can be assumed. To detect such a change, a discriminator compares the CSA-output with a given threshold.

The DC-output voltage depends on process parameters and leakage current and will vary from pixel to pixel. To be independent from this pixel to pixel variation, the discriminator is AC-coupled to the CSA. The principal realisation is given in Figure 4.18: The threshold voltage is set by the current I_{thr} and the resistor R.

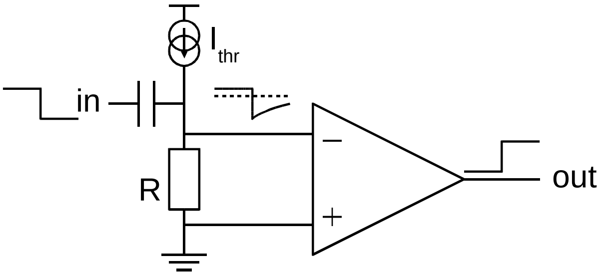

Figure 4.18 Principal of operation of a discriminator

The minimum voltage step, which should be detected, is determined by the noise. An equivalent noise charge of 25 electrons applied to a feedback capacitor of 0.5 fF would cause a mean noise signal of 8 mV. The threshold voltage of the discriminator should be several times larger than the noise contribution to avoid noise induced ghost-hits.

Due to threshold variation of MOSFETs, the differential amplifier drawn in Figure 4.18 can have an intrinsic offset of about 10 mV, which is of the same order as the threshold itself. So the effective threshold in each pixel varies due to the input voltage offset of the differential amplifier. To correct the threshold spread over the chip, one can either modify the threshold current I_{thr} or the resistor R. To modify the threshold in each pixel, current sources could be added in parallel with I_{thr} or resistors in series with R as shown in Figure 4.19. Via switches the additional current sources add a small current, which increases the threshold voltage. In the other case, additional resistors can be bypassed via switches lowering the threshold.

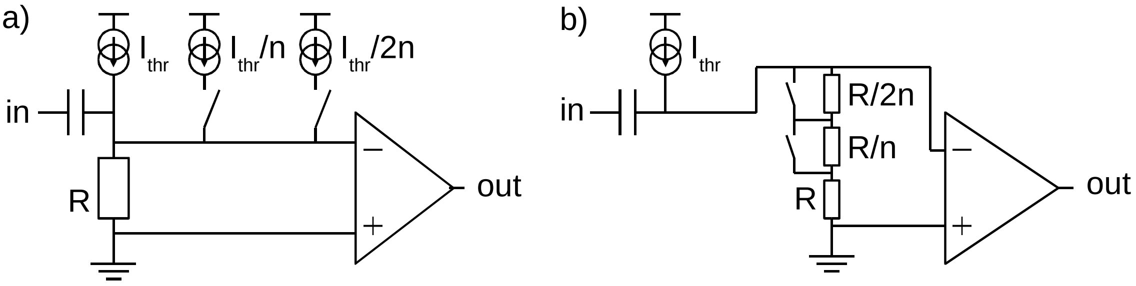

Figure 4.19 Principle of threshold modification with switches and resistors

Solution b) was chosen for the present design. As mentioned before, resistors needs a relatively large area. Therefore all resistors are substituted by transistors operating in the triode region.

The discriminator response is used by the pixel control logic to start the time measurement, enable the peak detector and notify a hit to the end-of-row and end-of-column logic to initiate the readout.

To avoid the relatively large coupling capacitor, the discriminator is implemented behind the differentiating stage of the shaper as shown in Figure 4.20.

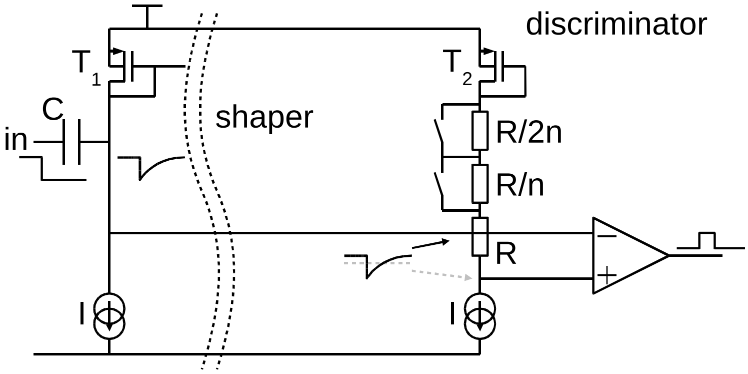

Figure 4.20 Discriminator implemented by using the shaper's capacitor

The layout of the shaper and discriminator combination is shown in Figure 4.21.

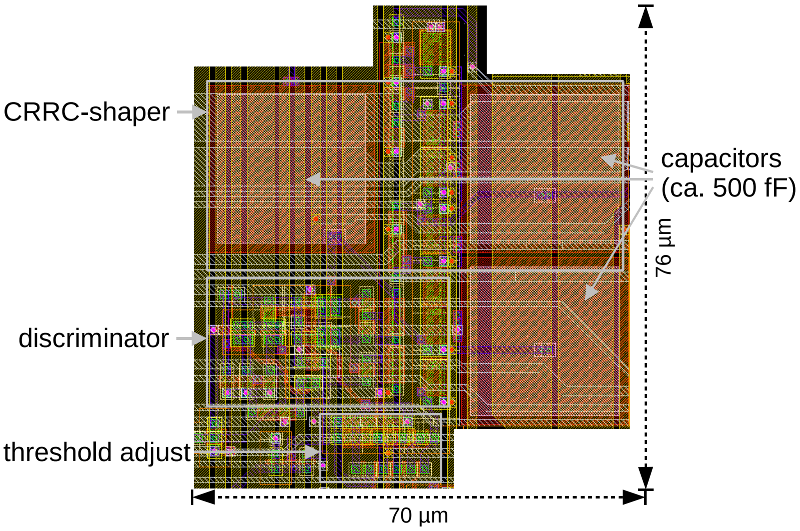

Figure 4.21 Layout of the CRRC-shaper and discriminator combination

4.5 Peak Detector

The extremum of the shaper output has to be sampled for readout. In triggered systems, where an external clock is available, usually sample and hold circuits are used. During a sample period the input voltage is traced, a subsequent hold signal instantaneously freezes the current voltage level. In a self triggering system a precise timing must be realised to send the hold signal exactly at the momentum of the peak. A smarter solution is achieved by using a peak detector, which automatically stores the extremum [Hor 89]. As shown in Figure 4.22 a simple peak detector can be formed by an ideal diode and a capacitor. The highest point of the input waveform charges up the capacitor, which holds that value while the diode is reverse biased.

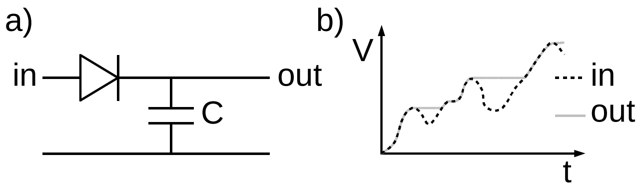

Figure 4.22 Simple peak detector and idealised behaviour

A main problems of this method is the voltage drop across a real diode, which makes the circuit insensitive to small peaks. Furthermore, the diode drop depends on temperature and current. Even a very high resistive load at the output of the peak detector would cause a discharge of the capacitor with time, falsifying the real peak level. To overcome these problems, feedback is used as shown in Figure 4.23. By taking feedback from the capacitor, the diode drop does not cause any problems. The additional unity gain buffer decouples any load from the storage capacitor.

In CMOS circuits no diodes are provided. Only parasitic diodes can be used, which are not well modelled. Usually diode connected MOS transistors are used. An

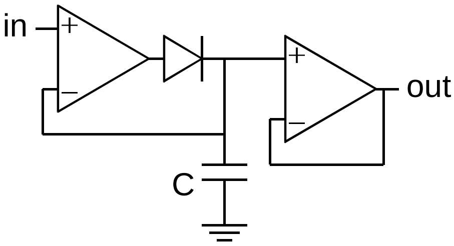

Figure 4.23 Improved peak detector with op-amps

alternative implementation, which also takes the negative polarity of the CRRC shaper output into account, is shown in Figure 4.24.

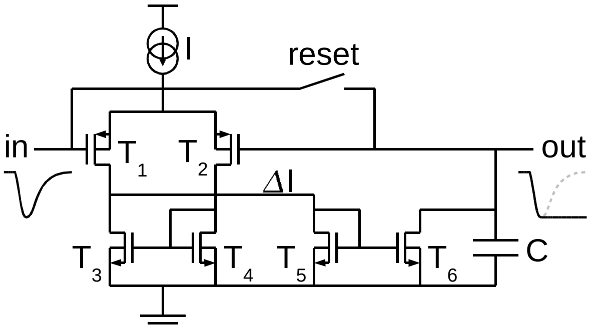

Figure 4.24 MOS implementation of a peak detector

Assuming the reset switch is closed. The output voltage is connected to the input. The capacitor is charged to the input level. With opening the reset switch the peak detector gets sensitive to peaks. As long as the input and output voltages are equal, the current I subdivides equally through T_1 and T_2. The current mirror $T_{3,4}$ exactly sinks this current. The current ΔI into T_5 is zero. No current is mirrored in T_6, so the voltage across the capacitor remains constant. As soon as the input voltage decreases (signal from the CRRC shaper output), the current through T_1 increases. As shown in Section 8.3.3 the current $\Delta I = dI_1 - dI_2 = -g_m \cdot dV_{in}$. The transconductance g_m is initially equal for T_1 and T_2. This current ΔI is mirrored via $T_{5,6}$ and discharges C until the output voltage is exactly the same as the input voltage. When the peak is reached, the input voltage rises resulting in a negative ΔI, which cannot be mirrored by $T_{5,6}$. As a consequence the capacitor C is neither discharged nor charged, keeping the value of the peak voltage. In practice the parasitic gate capacitances of $T_{5,6}$ have to be discharged by the negative ΔI, causing a short delay in switching of the current sink T_6. The omnipresent leakage current of the reset switch, implemented as a transistor, and T_6 slowly discharges the capacitor after peak detection. The larger C the smaller the discharging rate. On the opposite side a larger capacitor requires a larger current for a quick peak detection. As the current in the peak detector is only mandatory during peak detection, it is switched off for the rest of the time saving power.

The layout of the implemented peak detector is shown in Figure 4.25.

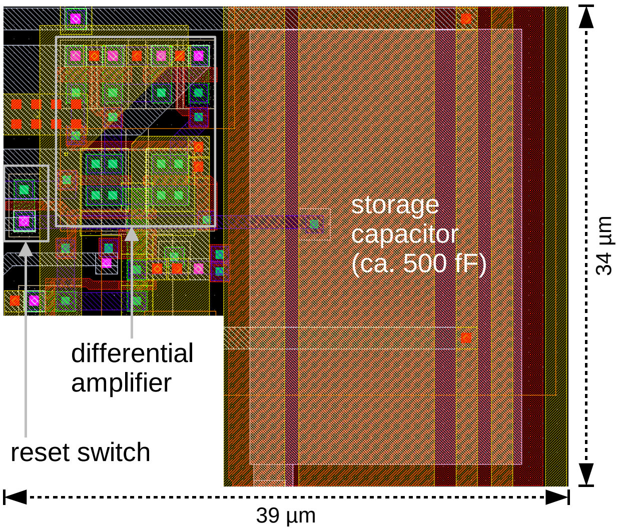

Figure 4.25 Layout of the implemented peak detector

4.6 Buffer

To avoid a discharge of the peak detector capacitor due to a current sinking load, the output of the peak detector must be buffered. As all pixels of a column are connected via a transmission gate to a common bus, the unity gain buffer must be able to drive the relatively large bus capacitance. A two stage amplifier is used as shown in Figure 4.26.

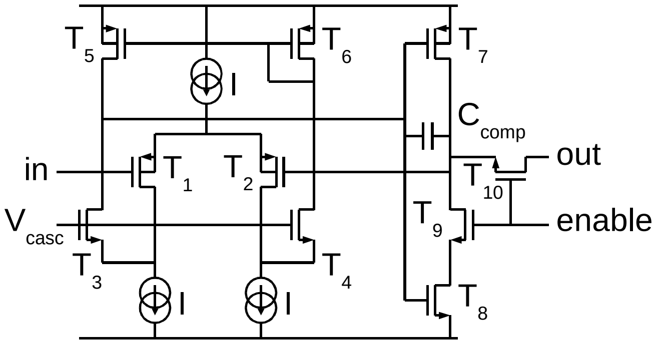

Figure 4.26 Output buffer in each pixel to drive a large capacitance

To provide the whole peak detector output range (down to ground), the first amplifier stage is a differential folded cascode configuration $(T_1 \ldots T_6)$. To drive the large bus capacitance and achieving the maximum output swing (rail to rail), two complementary common source amplifiers $(T_7,\ T_8)$ are used, which can provide the large current needed to change the large bus capacitance in a short time. Via an enable signal the output is connected to the bus. If the enable signal is off, the buffer is not only disconnected from the bus, but also the high current through $T_{7,8}$ is switched off to save power. A frequency compensation is realised by C_{comp}. The layout of the buffer is shown in Figure 4.27.

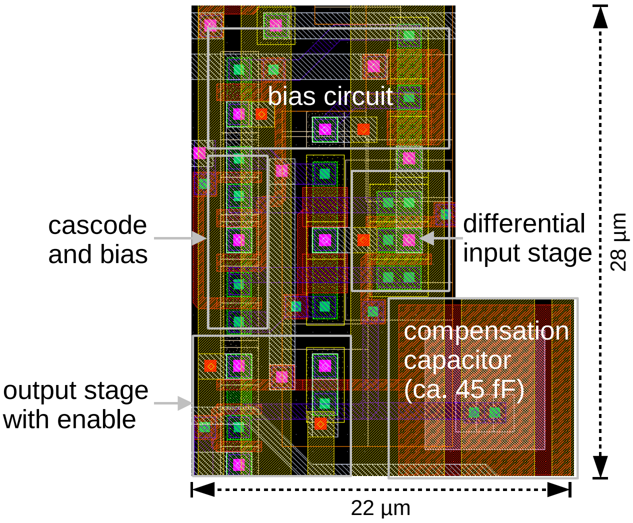

Figure 4.27 Layout of a buffer in a pixel

4.7 Pixel Control Logic

In each pixel a logic has to be implemented, which manages each block, reports a valid hit, controls the reset mechanism for the peak detector, starts and stops the time measurement and connects the pixel buffers to the readout bus. All these tasks are governed by the pixel control logic shown in Figure 4.28.

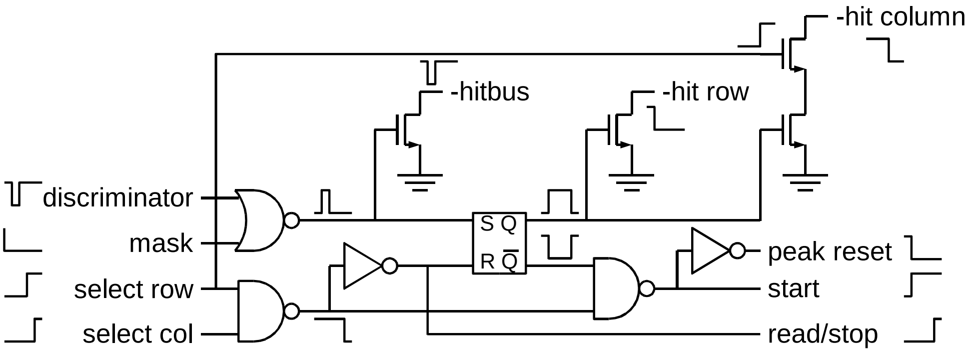

Figure 4.28 Pixel control logic

If the mask bit, which is provided by a shift register, is not set, the discriminator signal triggers an RS-flip-flop, which will not be reset until the pixel is selected for readout. The mask bit offers the possibility to switch off noisy pixels, which otherwise would paralyse the readout. For debugging the unmasked discriminator signal pulls down a hit-bus signal, which is routed out of the chip. The RS-flip-flop starts the time measurement, enables the peak detector and stores a hit until the pixel is selected. To select the pixel, a hit row signal notifies the end-of-row logic that a valid hit has occurred. The end-of-row logic selects successively every row, where a hit was recorded. In a selected row all pixels with a hit notify the end-of-column logic, which consecutively selects those pixels. A selected pixel distributes the read signal within the pixel to enable the buffers and to stop the time measurement. After a pixel has been read out and deselected, the peak detector is reset.

The layout of the pixel control logic is shown in Figure 4.29.

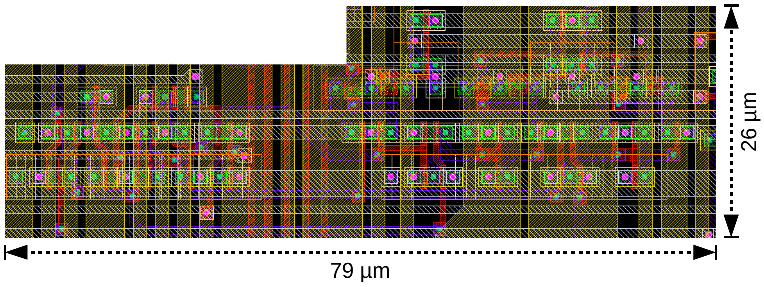

Figure 4.29 Layout of the pixel control logic

4.8 Time-to-Voltage Converter (TVC)

An off-line coincidence between a Compton scattering and a photo effect in different detector planes has to be achieved. Therefore the time between a hit and the pixel selection for readout has to be measured in each pixel. Usually the clock cycles of an external clock are counted during the interesting period. Assuming that the maximum time interval is 10 µs and a resolution of 1:100 (100 ns) is needed, the clock frequency has to be 10 MHz. Not only the use of a clock in a low noise environment is always crucial, but also the realisation of a seven bit (2^7=128) counter in each pixel is difficult. As discussed in I. Ibragimov's diploma thesis [Ibr 00], an analog approach is therefore adequate: For the interesting time period a constant current charges a capacitor as shown in Figure 4.30 a). The voltage across the capacitor (U_C) is proportional to the charging period t ($C\ U_C = I\ t$).

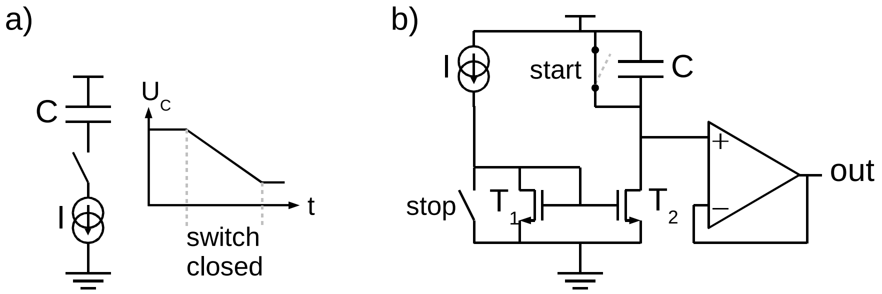

Figure 4.30 Time-to-voltage converter: a) simplified circuit (principal), b) a more practical solution

In b) a practical solution is presented: While the start switch is closed, the capacitor C is discharged. A start signal opens the switch initiating the charging of the capacitor via the current I, which is mirrored by T_1, T_2. A stop signal redirects the current I via another switch to ground so that no current is mirrored and the charging process stops immediately. The voltage across the capacitor is buffered by a subsequent unity gain buffer to achieve bus driving capability.

In the implemented version the unity gain buffer is substituted by a source follower and a pass transistor, which connects the buffer output to the bus for readout. For simplicity a simple source follower is used, which unfortunately adds a DC offset. The bus driving capability requires a relatively large current, which is only enabled during a readout cycle to reduce power consumption. A truncated layout (only part of the capacitor) is shown in Figure 4.31.

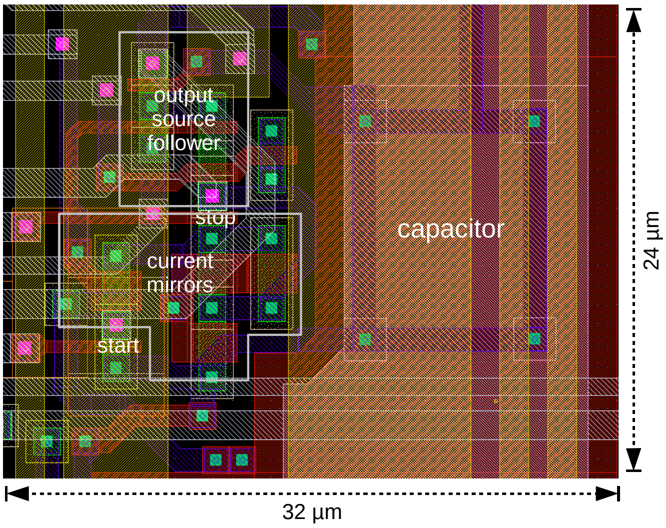

Figure 4.31 Truncated layout of the time-to-voltage converter

4.9 Pixel Shift Register

In order to control pixel related functions (threshold, mask bit, electrical injection and other debugging tools), a shift register meanders through all pixels. A shift register based on D-flip-flops, which are synchronously clocked, is shown in Figure 4.32.

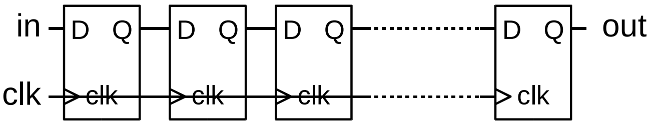

Figure 4.32 A shift register based on D-flip-flops

Care must be taken that the clock edges are sufficiently steep and that the clock delay (due to parasitic capacitances) from flip-flop to flip-flop is very short to avoid data losses. Therefore the clock is usually distributed in the opposite direction to the data. Intermittent clock buffers ensure sharp clock edges.

The realisation of a semi-static D-flip-flop is shown Figure 4.33.

In the clk=high state the memo is statically holding its value via the two inverters (Inv3, Inv4) and the output is the inverted memo value (Inv5). With the falling clk-edge Inv3 is disabled and Inv2 is enabled driving the memo line with the inverted input value. During this period the output of Inv5 is disabled and floating, which

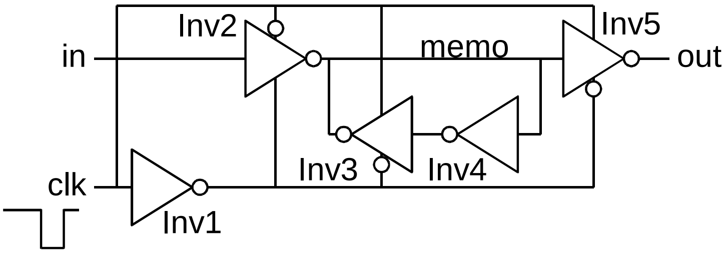

Figure 4.33 Realisation of a D-flip-flop

makes the D-flip-flop only semi-static. The very compact layout of one D-flip-flop is shown in Figure 4.34, which is designed to be directly connected to the next D-flip-flop to form a shift register.

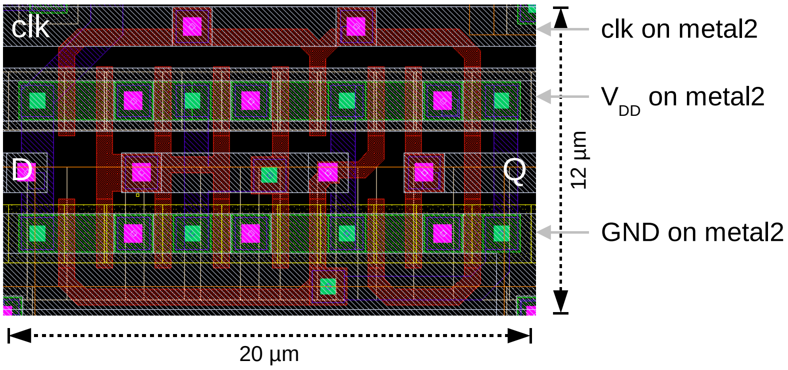

Figure 4.34 Layout of a D-flip-flop

Two D-flip-flops together with level shifters, used to assimilate the level for different supply voltages in the analog part and the digital part, are shown in Figure 4.35.

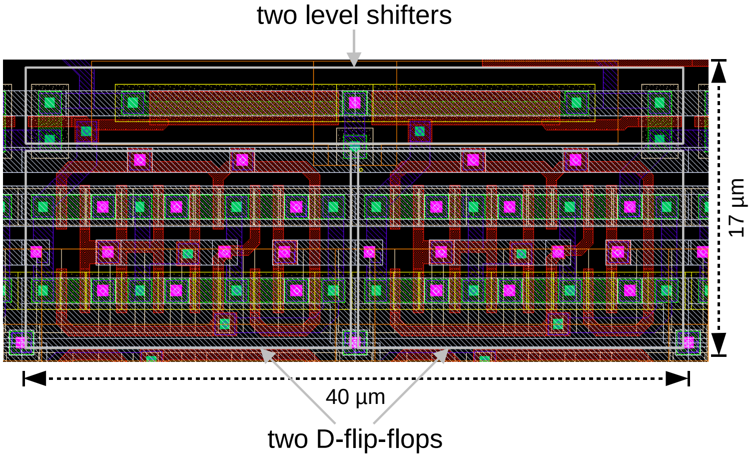

Figure 4.35 Layout of two D-flip-flops forming a shift register

4.10 Debugging

To trace some signals even if blocks of the readout chain fail, or to investigate single blocks, four analog signals of each pixel can be routed out off chip:

- CSA output signal
- CRRC-shaper output signal
- Peak detector output
- Voltage across TVC-capacitor

The number of simultaneously traced signals is limited by the two analog output buffers (see section 4.14.5). The signals are buffered by unity gain rail-to-rail buffers as described in section 4.14.5. The pixel, which is going to be monitored, and the buffer are selected by the pixel shift register.

4.10.1 Hit-bus

For a quick debugging, a hit-bus is implemented: An logical OR of all unmasked discriminator outputs is routed to a dedicated pad. The implementation of the 'OR' is shown in Figure 4.36: In each pixel an open drain NMOS signalises a discriminator hit. In the end-of-column a pull-up load provides a high state, if no hit in the column has occurred. The states at the pull-up load of all columns (-hitcol<x>) are combined in a similar way. If one state is low, the hitbus-line is pulled to the high-state. The hitbus-line is buffered and connected to the hit-bus pad.

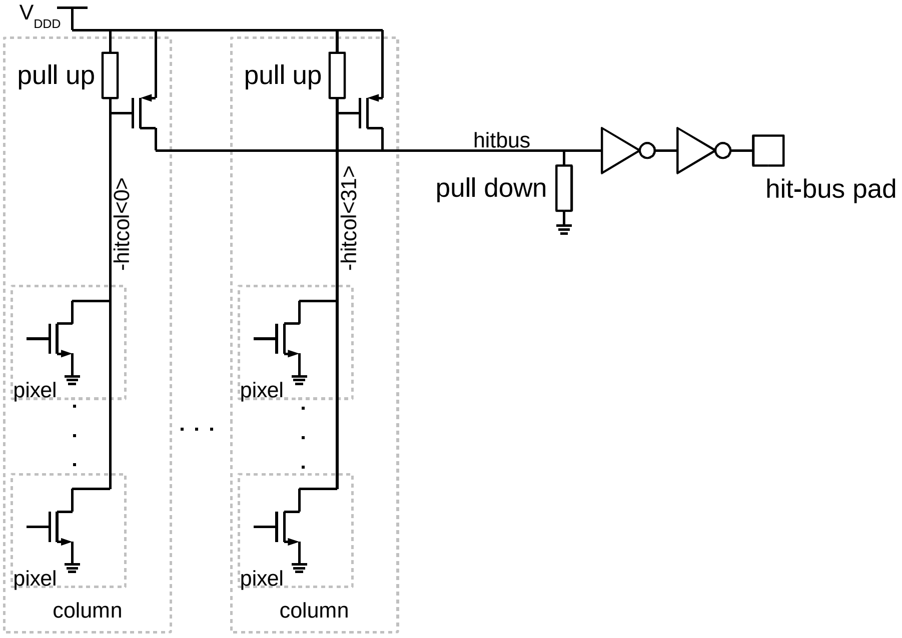

Figure 4.36 Implementation of the hit-bus logic

The pull-up loads and the pull-down load, drawn as resistors, are implemented as current sources. DAC 14 is used to set the value of these load currents. A disadvantage of this 'wired-OR' is the permanent current, flowing from V_{DDD} to ground, while hitbus is high. The advantage of the small number of components, particularly in the pixel, and the use of a single bus-line over the whole column, outweighs the disadvantage of permanent power consumption.

4.11 Complete Pixel

The layout of a complete (200 µm)^2-pixel is given in Figure 4.37.

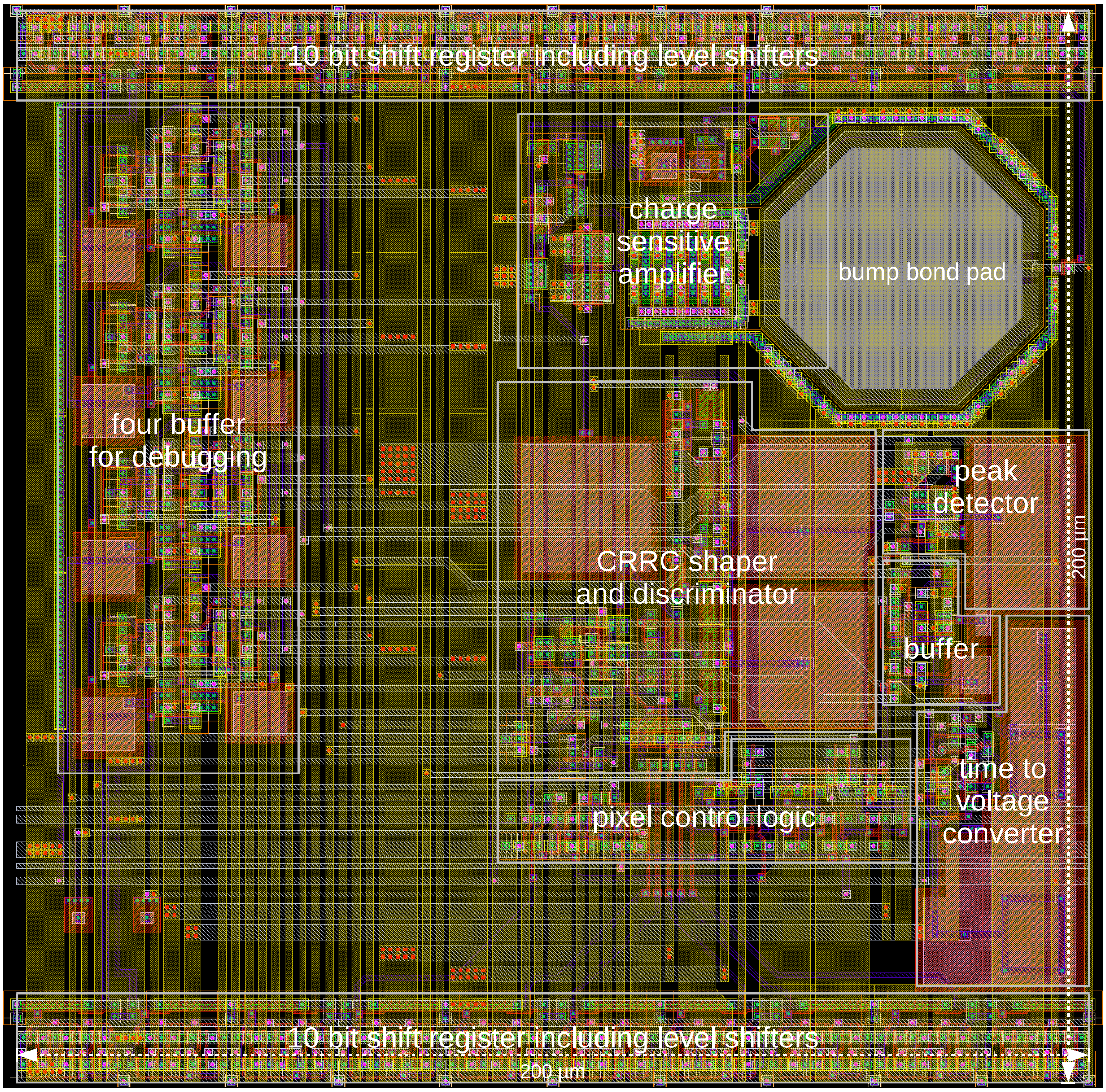

Figure 4.37 The layout of a complete pixel

4.12 Sparse Scan (End-of-Column/Row)

The first idea to scan a pixel matrix for valid hits is to select one pixel after another. To achieve a readout time of every pixel below 10 µs, a 100 MHz clock would be needed in a 1024 pixel matrix. As mentioned before, such a clock frequency introduces additional noise. As the occupancy in a pixel matrix is relatively low, a more sophisticated readout scheme is followed: Only a pixel with a valid hit is selected for readout. To reduce digital charge coupling, a minimum digital activity is achieved by a sparse scan, which scans only the respective rows and columns, which have registered a valid hit [Fis 99]. A block diagram and the time scheme are shown in Figure 4.38.

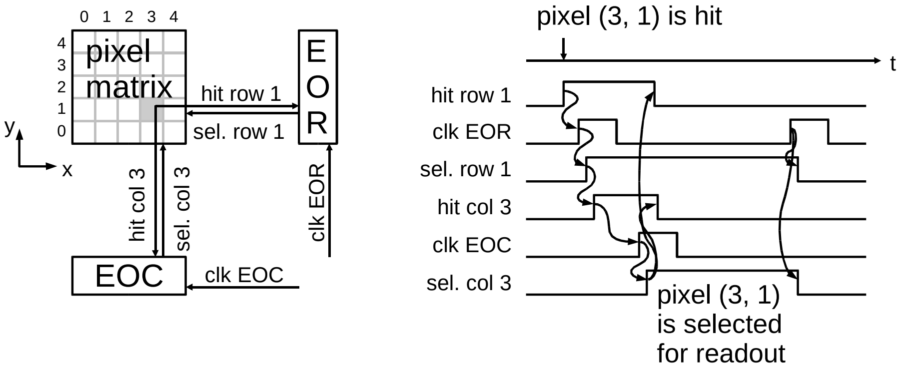

Figure 4.38 Principle of readout cycle responding to a hit

The realisation of the smart scan block, which is identical for the end-of-column (EOC) and end-of-row (EOR), is shown exemplarily for two input channels in Figure 4.39.

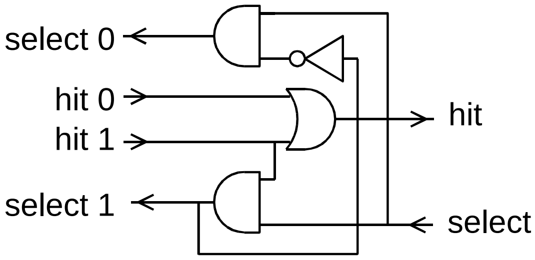

Figure 4.39 Base cell for end-of-column/-row block

If either 'hit 0' or 'hit 1' signalises a hit, the hit output flag is high. As soon as the block is selected, 'select 1' is set, if 'hit 1' is true. If 'select 1' is not valid, 'select 0' is set. To realise a monitoring of a complete matrix with 32 rows and 32 columns, a tree structure of several base cells has been implemented as shown in Figure 4.40.

The finally implemented base cells are slightly modified to permit a direct external addressing of each pixel for debugging purposes. An exhaustive use of inverting gates reduces the number of transistors and therefore saves area and increases speed due to lower propagation delays. This is also realised in the implemented base cells.

The EOR-logic and EOC-logic need different clock signals: As long as the EOC-logic reports a hit, an EOC-clock signal selects the next significant column. If no column in the selected row reports a hit (e. g. all pixels of this row with a hit has been successively selected), the next row has to be selected by an EOR-clock pulse. These signals are generated by a single external clock, which is adequately distributed. A dedicated clock-distribution circuit undertakes this task, which also considers an explicit external selection of a pixel as shown in Figure 4.41.

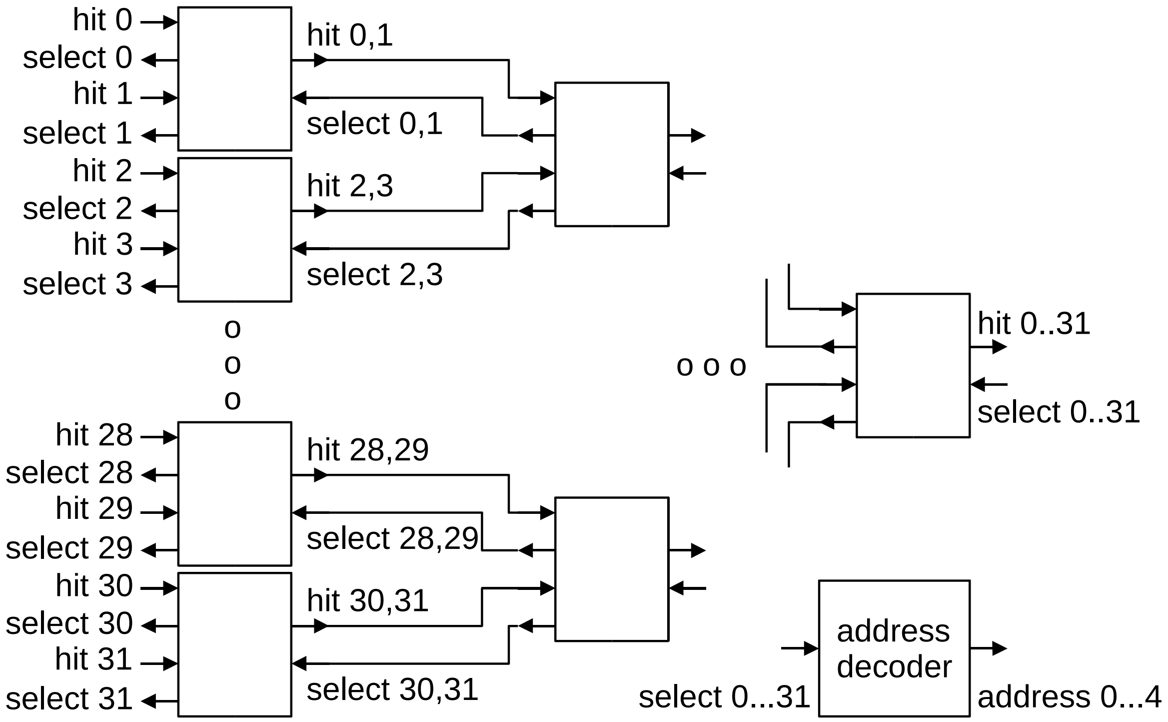

Figure 4.40 Propagation tree structure consisting of several base cells (see Figure 4.39) for 32 channels

Using the 'select' lines within the tree structure, additional logic encodes binary the address as shown in Figure 4.42.

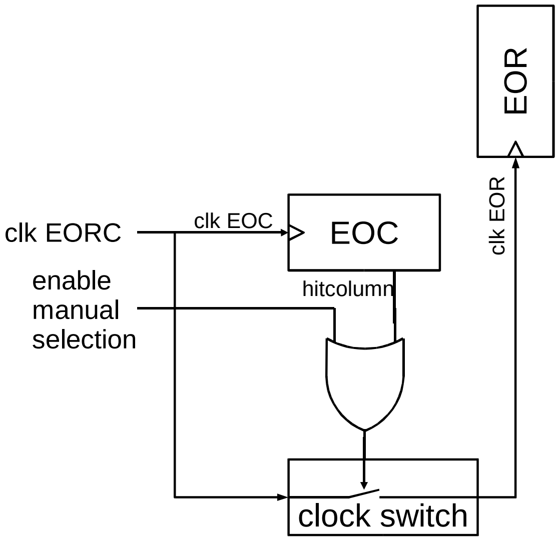

Figure 4.41 Clock distribution to EOC and EOR respectively

The clock-signals (clkEOR and clkEOC respectively) are used to propagate the select column/row signals of the tree structure via a flip-flop to the pixel matrix. At the same time, the address is stored in flip-flops to provide it to pads as shown in Figure 4.43.

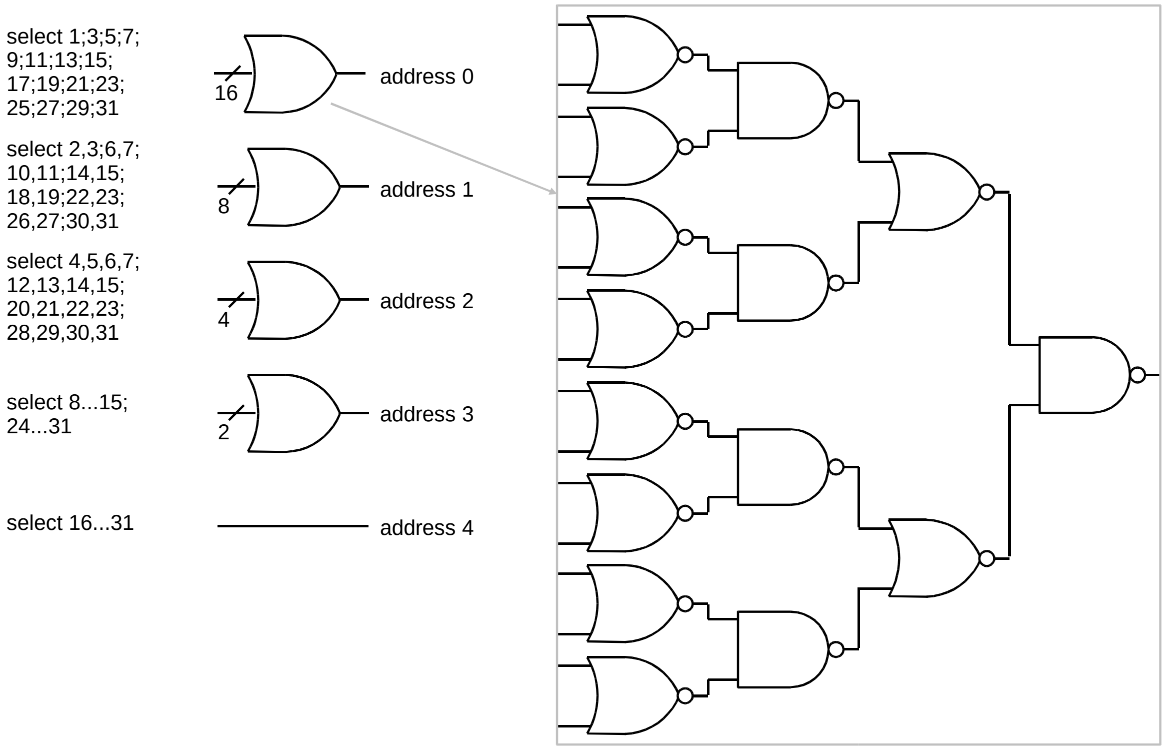

Figure 4.42 Schematic of address decoder and detailed view of the LSB-decoding

The pull-up termination transistors, which are biased by DAC 13, are also shown.

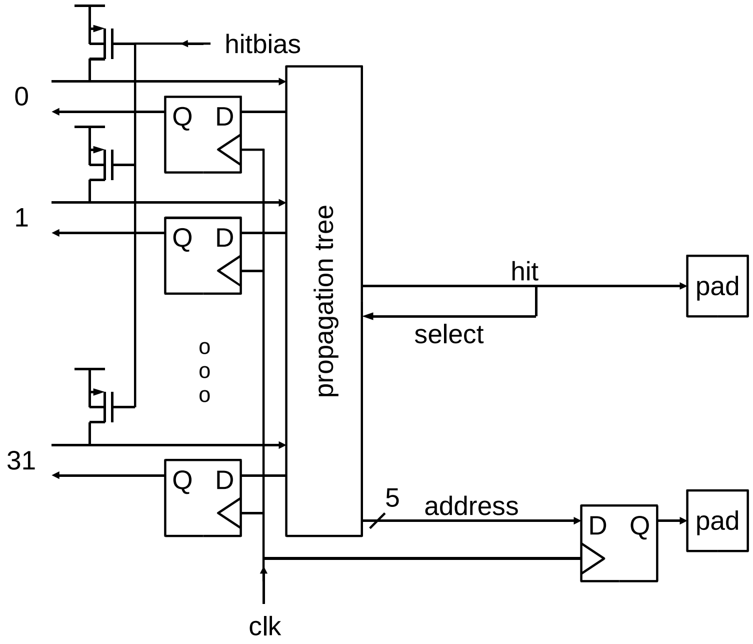

Figure 4.43 Latching the select lines and the decoded address
with a clock signal

A complete readout cycle is as followed: As soon as a hit appears in an unmasked pixel, the hit-row pad is set to '1' by the propagation tree of the end-of-row (EOR) logic. At the same time the input of the flip-flop, which addresses the row, in which a hit occurred, gets high by a back-propagation of the tree. The address is also decoded and provided to the address flip-flops. With a subsequent clk-signal all flip-flops shown in Figure 4.43 are triggered, selecting the row, which is chosen by the back-propagation tree, and latching the address to the output pads. Within the pixel, which has noticed a hit, of that selected row, the end-of-column (EOC) logic is notified (see section 4.7). The same procedure as in the EOR logic is repeated within the EOC logic. To select an arbitrary pixel, which has been hit, two clock pulses are needed.

4.12.1 End-of-Column Buffer

To buffer the analog signals (timing-information/energy-information), additional amplifiers are implemented in the end of column, which are enabled by the selection of a respective column.

To achieve an input range between ground and V_{DD}, two complementary folded cascode input stages are used as described in section 8.3.3. The full output swing is achieved by using a compensated rail-to-rail output stage. An unity gain configuration is achieved by negative feedback from the output. A block diagram is shown in Figure 4.44.

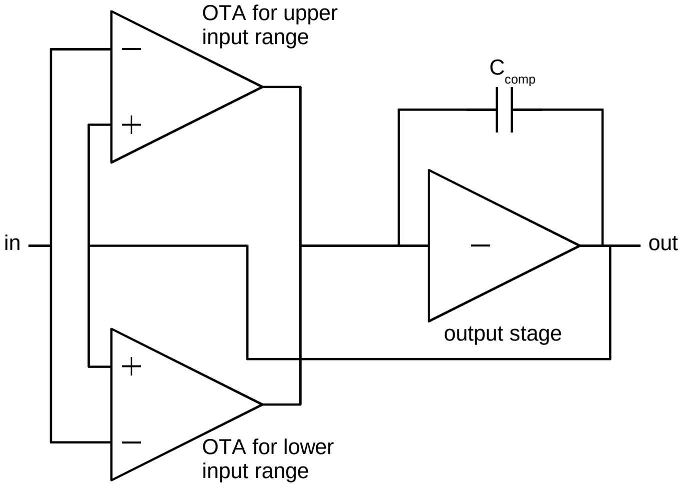

Figure 4.44 Complete block diagram of the analog output buffer

4.13 Current Sources

4.13.1 Digital-to-Analog Converter (DAC)

In each pixel 11 different currents are needed, in the periphery four. In the first version of the chip these 15 currents were supplied by external current sources. In the last version, the currents are adjustable on the chip to overcome process variations, simulation deficits and changes in the environment. To achieve this, a digital information has to be converted into an analog current by means of a digital-to-analog converter (DAC).

A simple current DAC is realised by switching different multiples of a reference current to a summing point as shown in Figure 4.45.

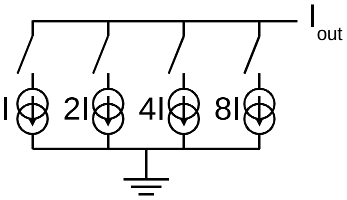

Figure 4.45 Simple current DAC

In practice care must be taken to avoid errors due to Early effect and mismatch of current mirrors. An cascoded approach to generate the bias voltage $(V_{ref0...3})$ for the current mirrors is shown in Figure 4.46. The cascode voltages V_{cascP} and V_{cascN} are supplied by the current reference circuit (see Figure 4.53).

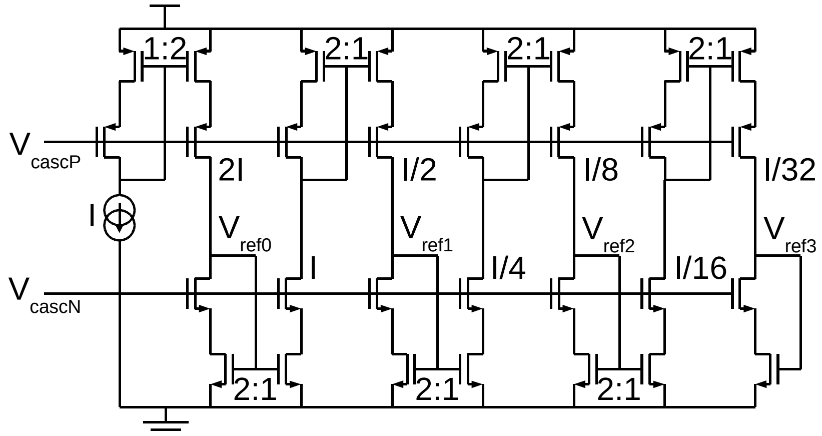

Figure 4.46 Generating reference voltages for the current mirrors in the DAC

The reference voltages are then used to generate currents in matched transistors. By switching these currents via NMOS pass transistor, the corresponding current is generated. The implemented DAC cell is shown in Figure 4.47.

The digital DAC code is provided by a latch, which is loaded by an external load signal with the data provided by a shift register. Two additional bits are used to switch the current completely off (pull the gate of the output current mirror to V_{DDA}) or switch to a power supply voltage dependent maximum current (pull the gate of the output mirror to GNDA). A total number of 10 bits is therefore needed to program each DAC.

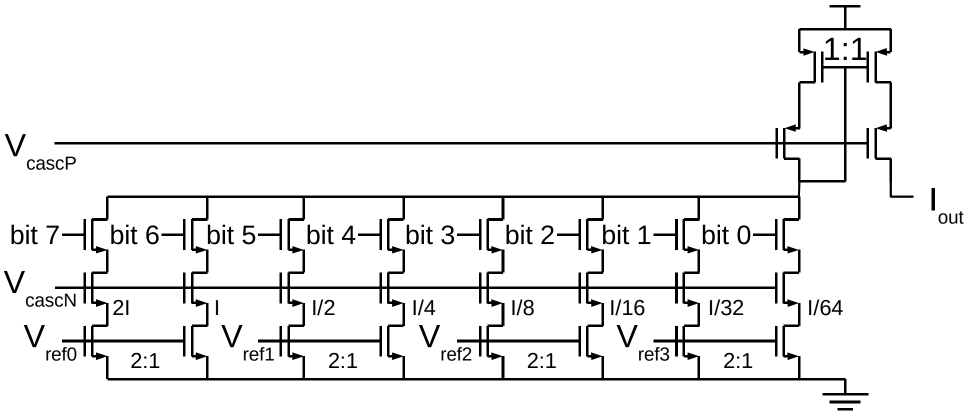

Figure 4.47 Cascoded current mirror with pass transistors in the DAC

A level assimilation between the different supply voltages in the analog part and the digital part is achieved by an interfacing level shifter.

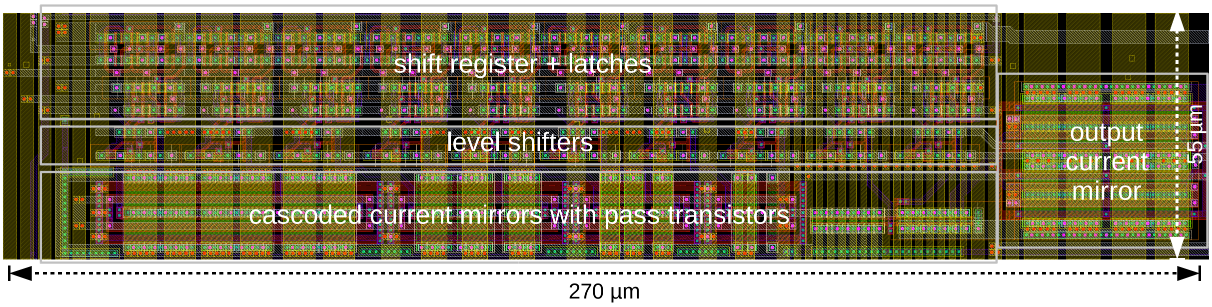

Figure 4.48 Layout of one DAC-cell

The layout of one DAC-cell including the shift register, the latch, the level shifters and the cascoded current mirrors is shown in Figure 4.48.

To generate all 15 currents, a corresponding number of copies of this cell is implemented. An implemented analog multiplexer leaves the choice to measure the current of maximal two arbitrary selected DACs externally or to impose an external current (see section 4.13.3).

Each DAC is designed to source a current of up to almost four times the reference current ($I_{ref,design}$=50 µA). To realise a different current range or to sink a current, a subsequent current mirror with an appropriate ratio must be realised. Table 4.3 lists the DAC-numbers as implemented, their functions, the default values and the calculated current in each pixel.

DAC number	DAC name	function	default DAC setting	current mirror ratio	I_{pixel} [nA]
0	sfbias	source follower bias of TVC	50	1:16	1890
1	tbias	current to charge capacitor in TVC	50	1:64	480
2	bufbias	bias current for analog pixel buffer and debug buffer	250	1:64	2400
3	peakbias	bias for peak detector	200	1:16	7700
4	feedbias	bias for DC-feedback of CSA	0	1:128	50
5	vsf	source follower bias of CSA output stage	50	1:64	475
6	vtau	time constant of CRRC-shaper	50	1:96	110
7	vthr	analog threshold of discriminator	0	1:32	0
8	discbias	bias current of discriminator	100	1:64	960
9	vlast	active load in CSA/regulated cascode bias	100	1:64	960
10	vinpbias	bias of the input transistor in the CSA	250	1:4	37870
11	icommonS	bias for analog buffers (pad/EOC)	50	1:1	not mirrored into pixel
12	icombias	bias for analog buffers (pad/EOC), set as 11	50	1:1	
13	hit-row/ -col bias	load current for wired-OR of hit column/hit row	50	1:1	
14	hit-bus bias	load current for wired-OR of hit-bus	0	1:32	
15	NC	no connection	0	1:1	

Table 4.3 DAC functions and properties

The reference current needed to generate the bias voltages in Figure 4.46 can either be applied externally or generated internally by a reference cell.

4.13.2 Thermal Voltage Referenced Self-Biasing

A reference current is needed in the DAC. To generate such a current, a simple resistor can be used, which generates a defined current from the supply voltage as shown in Figure 4.49.

The current I through T_1 is mirrored into T_2, which can be used as a reference current. To evaluate the current, the gate source voltage of T_1 in equation 8.7 has to be substituted by $V_{DD}-R\cdot I$. Solving for I yields:

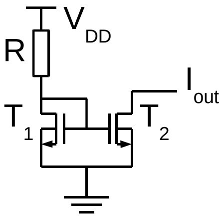

Figure 4.49 Simple current generation

$$I=\frac{V_{DD}-V_{thr}}{R}-\frac{1}{R^2\beta}\left(\sqrt{1+2R\beta(V_{DD}-V_{thr})}-1\right) \tag{4.48}$$

A disadvantage of the simple current generation is its strong supply voltage dependence, which can be overcome by a thermal voltage referenced self-biasing as shown in Figure 4.50.

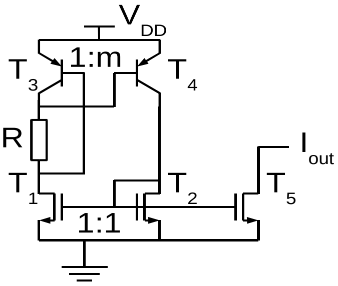

Figure 4.50 Thermal voltage referenced self-biasing

Via T_1 and T_2 the same current is mirrored through the bipolar transistors T_3, T_4. As T_4 is m-times larger than T_3, the base-emitter voltage needs to be smaller to sink the same current. The difference of the base-emitter voltages drops across the resistor R and sets the current.

The collector current I_C of a bipolar transistor as a function of its base-emitter voltage V_{BE} is given by

$$I_C=I_S e^{\frac{V_{BE}}{n V_T}} \quad \text{with} \quad V_T=kT/q \tag{4.49}$$

The saturation current I_S (typ. fA) and the emission coefficient n (typ. about 1, in the given process $n \approx 1.48$) are process dependent parameters. Solving for V_{BE} yields:

$$V_{BE}=n V_T \ln\frac{I_C}{I_S} \tag{4.50}$$

The current now is given by the voltage drop across the resistor:

$$I=\frac{\Delta V}{R}=\frac{V_{BE3}-V_{BE4}}{R}=\frac{n V_T\left(\ln\frac{I_C}{I_S}-\ln\frac{I_C}{m I_S}\right)}{R}=\frac{n V_T \ln m}{R}=\frac{n k T}{q R}\ln m \tag{4.51}$$

Theoretically the current is completely independent of the supply voltage and of process parameters like threshold voltages or the saturation current I_S, but is proportional to the absolute temperature. If temperature independence is required, a bandgap referenced biasing [Bak 98] can be used. Assuming an ambient temperature of 25 °C the current is within a 10 % deviation between −5 °C and 55 °C, which is satisfactory in the present design since the individual current can be adjusted by the DAC settings. A better precision of the reference current during development cannot be achieved since the processing tolerance for resistors is only guaranteed within 15 %.

In a simple CMOS process no dedicated bipolar transistors are provided. A parasitic lateral bipolar transistor can be used instead as shown in Figure 4.51. The p^+-regions in the n-well, which usually form the source and drain of a PMOS, form the emitter (E) and the collector (C) respectively. The lightly doped n-well forms the base between emitter and collector. Usually the bulk has the highest potential switching off the parasitic bipolar transistor completely. So it plays no role in standard CMOS circuits, but by pulling down the bulk, the parasitic pnp-transistor starts conducting.

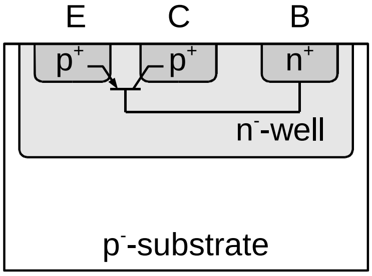

Figure 4.51 Parasitic lateral bipolar transistor in an n-well CMOS process

A well known problem of bias cells is the fact that they provide two stable states: One is the state, in which the correct reference voltage is generated. In the other stable state no current is generated at all. All transistors are non-conductive. To avoid this state, a start-up circuit has to be implemented as shown in Figure 4.52.

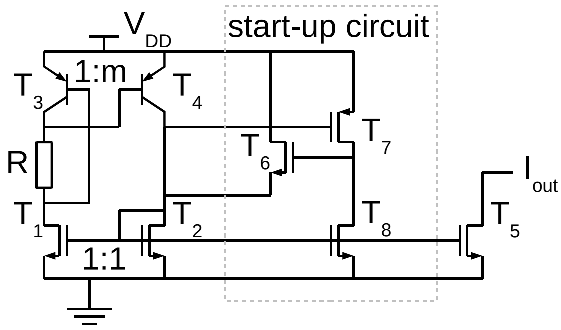

Figure 4.52 Reference circuit with start-up

In the case, when no current flows, the gate source voltage of T_2 must be zero. The long PMOS T_7 pulls the gate of the source follower T_6 to V_{DD}. As a consequence the gate of T_2 is pulled to a higher voltage causing a current flow in $T_{1,2,8,5}$. If the current exceeds a certain limit, given by the length of T_7 and the supply voltage, the transistor T_8 switches T_6 off by pulling its gate to ground. Once a certain current is generated, the circuit approaches the intended current reference.

It is known that the bipolar transistors have a relative large Early-effect. This results in a slight voltage dependent reference current. To reduce this effect, all transistors, not only the bipolar transistors, are cascoded ($T_{9...15}$) as shown in Figure 4.53. Furthermore, two cascode voltages (V_{cascN}, V_{cascP}), which are needed in the DACs, are generated.

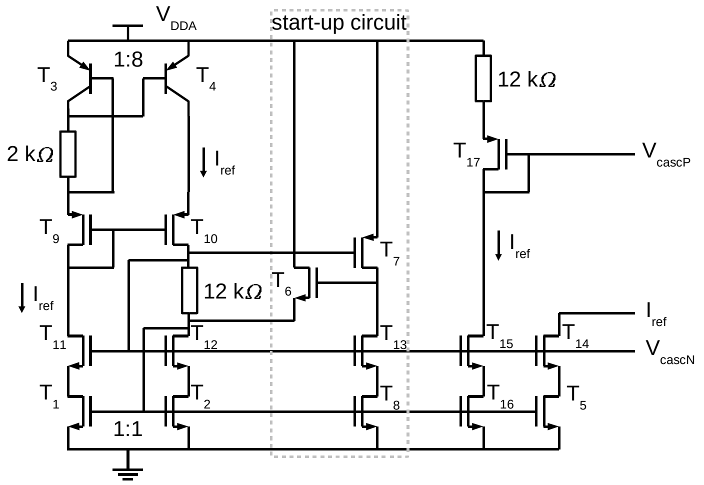

Figure 4.53 Implemented reference circuit

The cascode voltages are generated by a serial connection of a diode connected transistor and a resistor. The voltage drop across the resistor must be larger than the saturation voltage of $T_{1,2}$. A reference current of 50 µA causes a voltage drop of 600 mV across the resistor (R=12 kΩ), which is sufficiently large to keep T_1 and T_2 in saturation.

The reference cell is the only cell, in which resistors are used on the chip core. A layout of the reference cell is shown in Figure 4.54: A ratio of 1:8 (m=8) between the bipolar transistors has been realised.

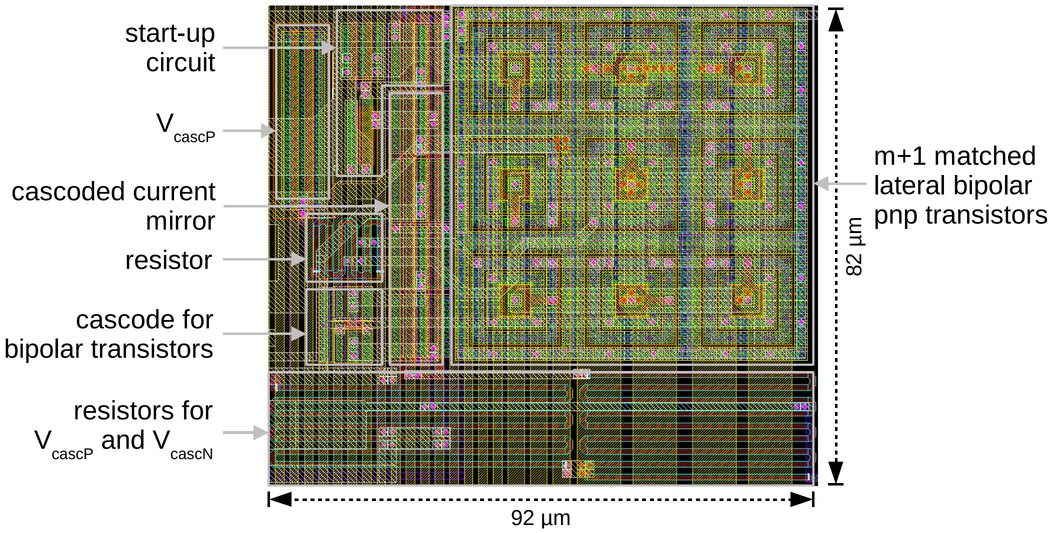

Figure 4.54 Layout of the thermal voltage referenced self-biasing circuit

4.13.3 Current Monitoring

To monitor maximal two arbitrary currents or impose external currents, an analog multiplexer is implemented to route the DAC outputs to monitoring pads (IMON). The principal of the circuit and the implementation is shown in Figure 4.55. Via the shift register (IMUXSR) the state of the multiplexers is selected. Either the monitoring pads are bypassed or intermit the DAC current path to the current mirror. If the current path is intermitted, then the current can be measured externally by a current meter (e. g. SourceMeter).

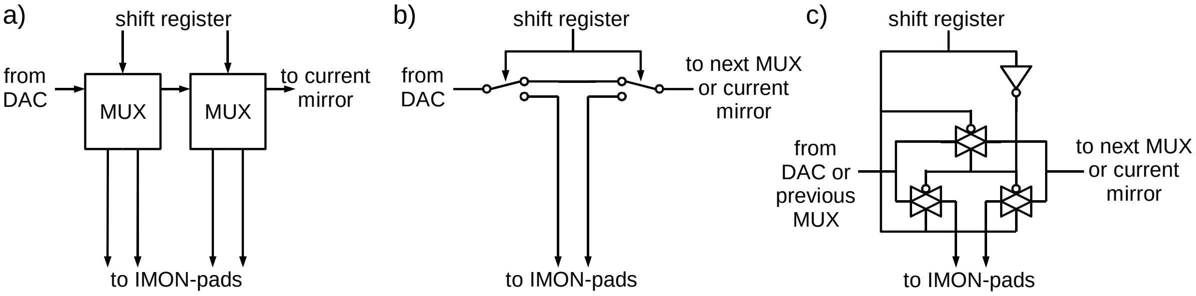

Figure 4.55 Current monitoring circuit: a) block diagram with two MUXs, b) principle of each MUX, c) implementation of a MUX with transmission gates

Since all MUXs are commonly connected to the IMON-pads, DAC 15 (no function) can be used to add additional current to a selected DAC output, if the IMON-pads are shorted. Alternatively, DAC 15 can be used to generate an external voltage across a load resistance to provide the analog voltage for an analog threshold adjustment of the discriminator.

Care must be taken as the IMON-pads are intentionally[21] not protected. A marginal protection is given by the small source-bulk diodes of the transmission gates.

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[21] If a relatively large current is going to be imposed, then maybe a higher voltage than the supply voltage has to be applied.

The layout of the current multiplexer is shown in Figure 4.56.

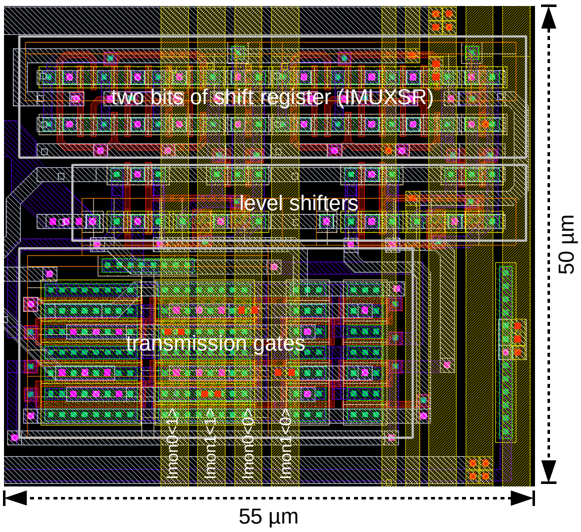

Figure 4.56 Layout of the current multiplexer

4.14 Communication Interface (Pads)

Once the core of a chip has been designed, the communication to the off-chip electronic must be ensured. Therefore connections providing the power supply and connections for in-/output must be designed. Beside the digital input and output, which does the communication to the digital circuitry (set shift registers, provide clocks, read column/row addresses of pixels), the analog output of the analog levels is the dominant challenge.

4.14.1 Power Supply Pads

Various power supplies have to be applied to the chip:

- Analog power supply:
  V_{bulk}: Bulk contact of the input FETs in the CSA
  V_{DDA}: Positive analog supply voltage ($V_{DDA} \leq V_{bulk}$)
  V_{CCA}: Auxiliary voltage for the CSA ($GNDA \leq V_{CCA} \leq V_{DDA}$)
  $GNDA$: Analog ground
- Digital power supply (separated from analog supplies to avoid crosstalk):
  V_{DDD}: Positive digital supply voltage
  $GNDD$: Digital ground
- Substrate contact:
  GND: All NMOS bulk contacts are connected to the substrate
- Buffer supply:
  V_{DDABUF}: Positive supply voltage of analog output buffers
  $GNDABUF$: Ground of analog output buffers
  V_{DDDBUF}: Positive supply voltage of digital input and output buffers
  $GNDDBUF$: Ground of digital input and output buffers

Due to the large number of different power supply pins, a full custom layout of all pads has been made. All Pads are connected to a common wide supply bus, which is routed over relatively large capacitors (2×3.4 pF per pad) used to block all power lines against spikes.

4.14.2 Digital Input Buffer

Input Buffers are used to protect the chip against electrostatic discharge (ESD). A MOS-input practically has an infinite resistance and a relatively small capacitance. Depositing a small charge, e. g. by touching the input with the human body, a large voltage would arise on the small capacitance, destroying the thin oxide underneath the gate. To avoid this kind of damage, protection diodes are used to dissipate charges, if the applied voltage exceeds the supply limits, i. e. raises above the positive supply voltage or drops below the ground level.

In the implemented input buffer 15 diodes[22] protect each input pad against ESD. V_{DDDBUF} is used as the positive supply voltage.

To define a default input level even if no external signal is applied, e. g. a bond connection is missing, or to simplify probing before bonding, a pull up or pull down mechanism is implemented: A long transistor operating in the triode region provides a designed resistance in the order of 200 kΩ for a supply voltage of about 3 V. The resistance pulls the input to $GNDD$ or V_{DDD} respectively.

A simplified schematic is shown Figure 4.57. Beside the protection and pull-up circuitry, two inverters are implemented to ensure correct logic levels and fast rise- and fall-times respectively.

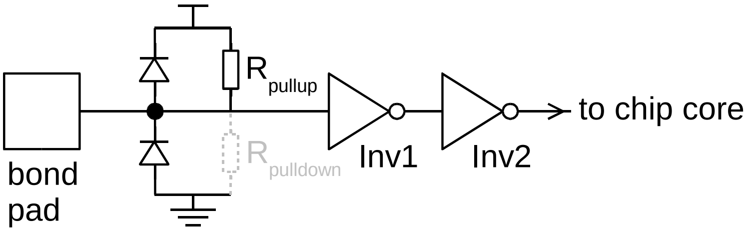

Figure 4.57 Simplified schematic of a digital input buffer

4.14.3 Digital Output Buffer

The chip must be able to drive a relatively large capacitance and a low resistance, for instance the input of the external logic (field programmable logic, FPGA from XILINX™) or the probe of an oscilloscope (1 MΩ || 10 pF). Parasitic capacitances are added from lines on printed circuit boards (PCB) or cables.

To charge a capacitance of 10 pF within 1 ns up to 1 V, the large current of 10 mA must be provided. The switching transistors must be able to cope with such currents, which results in large area transistors. These transistors form again a capacitance, which has to be charged. A sequence of buffers (with increasing driving

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[22] The number of diodes was adapted from the standard pads to sink a sufficient current in case of ESD.

capability) is needed to drive a relatively large off-chip capacitance with the low currents provided inside the chip core.

A simplified schematic including the output protection is shown in Figure 4.58. The protection diodes are used to suppress reflected signals from unterminated transmission lines.

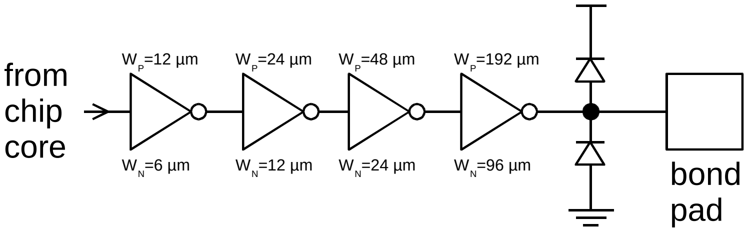

Figure 4.58 Simplified schematic of a digital output buffer

Particularly in the layout of the output pads care must be taken to avoid latch up by the use of dedicated guard ring structures (see section 8.2).

4.14.4 Clock Distribution for Shift Registers

Five shift registers inside the chip must be fed with data. Each shift register needs a clock and data input and provides a data output to verify its functionality. In total 15 digital input/output pads would be needed to control five shift registers. Here another approach was made, which uses a dedicated shift register to select the shift register to be loaded by an appropriate clock distribution as shown in Figure 4.59.

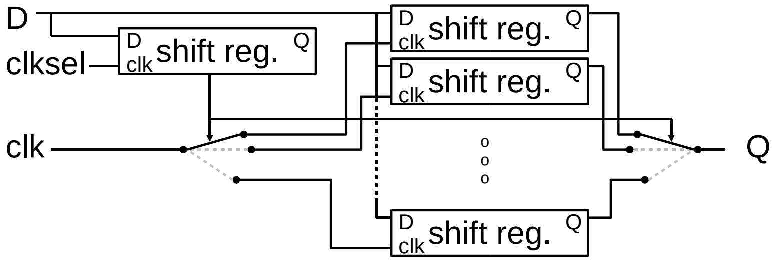

Figure 4.59 Clock distribution via an additional shift register

By applying a clock at the clksel input, the data from the D-input are shifted into the shift register controlling the switch, which distributes the clk-signal to one of the drawn shift registers. At the same time, the output Q of the selected shift register is connected to the output Q.

Only four lines are used to control an arbitrary number of internal shift registers. In the implemented design five internal shift registers are used. One state of the select shift register is used to provide the end-of-column/end-of-row clock. The function of the different states and the corresponding shift register properties are shown in Figure 4.3.

number of shift register	name of shift register	length [bits]	function
0	DACSR	160	to set DAC values (10 bit/DAC)
1	IMUXSR	32	to route current of DACs to monitor pads (IMON)
2	AnalogOutSR	14	to select the analog output signals and the size of the compensation capacitor
3	not used		
4	not used		
5	PIXELSR	1280	to store the settings of 64 pixels and to route the debugging buffers
6	EORC	0	no shift register; used to distribute the clock for readout of EOR/EOC
7	EORCSELSR	10	to select a pixel manually

Table 4.4 Shift register number in the select shift register and properties of the other shift registers

4.14.5 Analog Output Buffer

The internal analog levels providing the timing information and the detected energy are converted externally by a successive approximation analog-to-digital converter (ADC). To drive the input capacitance of the ADC or any external oscilloscope probe (1 MΩ || 10 pF), an analog output buffer is needed.

In a first step two simple source followers were used, which were biased by an external resistor as shown in Figure 4.60.

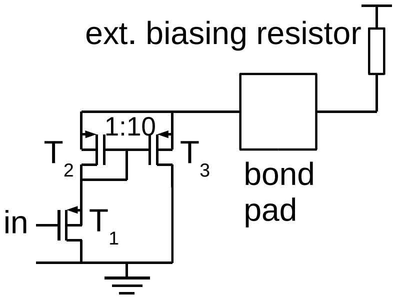

Figure 4.60 Source follower to drive external load

The externally applied current splits 1:10 through the transistor $T_{1,2}$ and T_3 respectively. The source of T_1 follows the input signal and drives a second source follower T_3. The output therefore follow the input voltage with a DC offset. While using PMOS-transistors, which are electrically isolated in their own n-wells, an external voltage higher than the internal power supply can be used to reproduce the full input swing.

The DC-offset introduced by the two source followers and the deficit of an output voltage depending biasing owing to the use of a biasing resistor instead of a current source ask for a more sophisticated output stage. An unity gain buffer without or with a negligible DC-offset and both an input and output range between ground and the supply voltage has been designed.

To achieve an input and output range between ground and V_{DD}, an arrangement as described in section 4.12.1 has been realised with a four times larger output stage to drive the relatively large external load. To provide a large driving capability, the output stage consists of broad transistors (W_P/L_P=120/0.6, W_N/L_N=40/0.6) resulting in a relative high power consumption: Using equation 8.53 an estimation of the power consumption is given in table 4.5.

V_{DD} [V]	3.0±0.05	4.0±0.05	5.0±0.05
I [mA]	2.0±0.05	5.8±0.05	11.7±0.05
P [mW]	6.0±0.2	23.2±0.4	58.5±0.6

Table 4.5 Evaluated power consumption of the analog output stage

The compensation capacitor in the output stage can be switched off or reduced to half the design value via a shift register to achieve a faster slew rate, but then the circuit tends to oscillate.

4.14.6 Debugging Features

In contrast to discrete electronic circuits on printed circuit boards, where probes can be attached to any arbitrary conducting path for debugging, in integrated circuits different functions for probing must be implemented in the design itself.

Via additional shift registers, multiplexers and buffers a programmable routing can be used to view several signals inside the chip core. In each pixel the CSA output, the CRRC output, the peak detector output and the voltage across the TVC-capacitor can be selected to be routed to an analog output buffer (see section 4.10). Therefore in each pixel additional analog buffers have been implemented, which can be enabled by appropriate programming of the pixel shift register. Care must be taken that only one analog buffer of each type is selected at the same time to avoid a short between two drivers.

Some additional voltages (cascode voltages V_{cascP}, V_{cascN}, the power supply voltage on the chip (V_{DDA}, V_{CCA}, V_{DDD}, V_{bulk}, etc.), reference voltages for the DAC ($V_{ref0...3}$) and the DAC-output voltages) should be monitored. As the analog output buffer wastes a lot of power, only two buffers are implemented, which are driven by multiplexers. The multiplexers are controlled by a shift register and select one out of 32 arbitrary lines. The two multiplexers are cross-coupled to permit an access to any signal, even if one analog output fails. Beside the debugging voltages and signals the energy information and timing information of a pixel can be selected.

5 System Setup

The chip has been fabricated in a multi project wafer (MPW) run through Europractice IC Service[23] at Austria Micro Systems (AMS). To test the performance of the chip, a test environment as shown in Figure 5.1 has been set up.

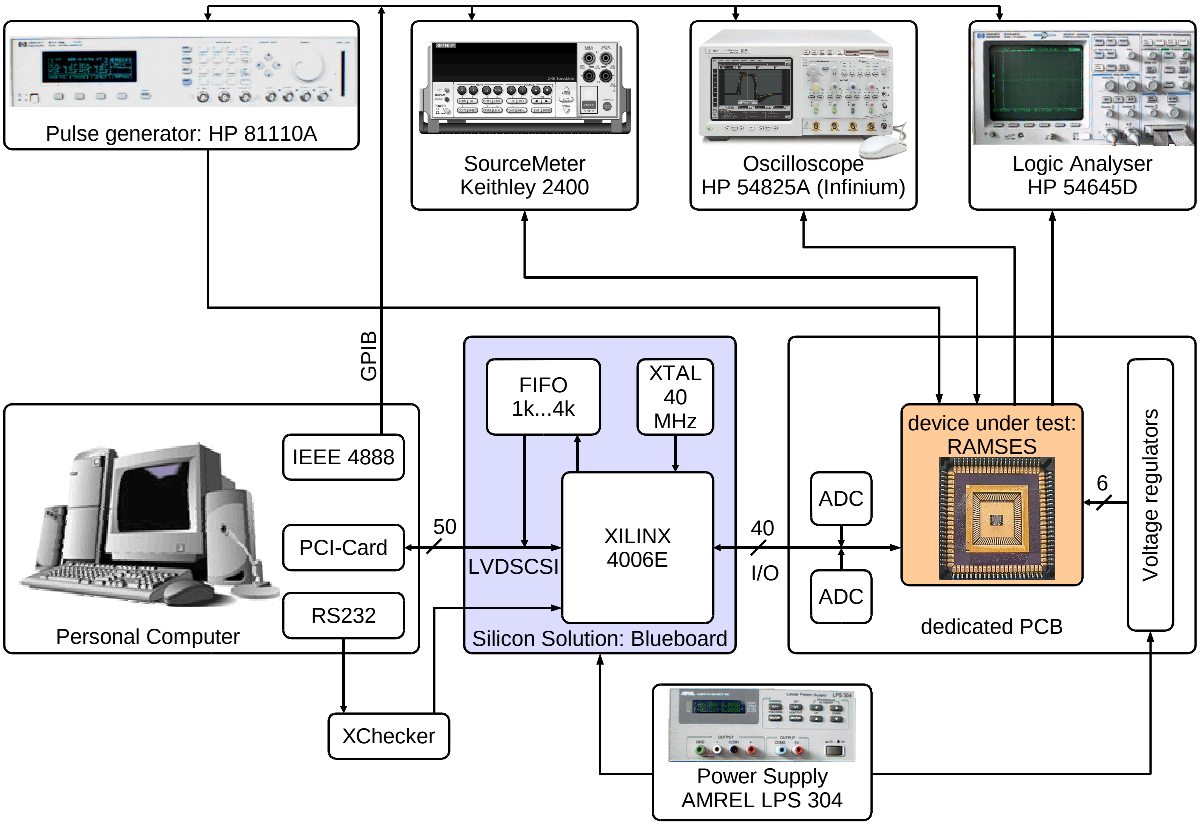

Figure 5.1 Overview of the test environment

The device under test (DUT) is situated on a dedicated printed circuit board (PCB, see section 5.1), which also provides all needed regulated voltages (adjustable voltage regulator LM 317). The analog information is directly converted nearby the chip by two 12-bit successive approximation analog-to-digital converters (ADCs) from Texas Instruments (ADS 7818E, 0.5 MHz throughput rate). To provide control signals to and read data from the DUT, a field programmable gate array (FPGA) from XILINX™ manages the whole communication on a Blueboard from Silicon Solutions. A FIFO buffers the ADC-values and timing information for the readout. A quartz crystal (XTAL) is used to generate the timing information inside the XILINX™ and provide the ADCs with clock signals. The control and readout of the Blueboard is done via a 50 wire low voltage differential cable (LVDSCSI) and a dedicated PC-card (PCI or ISA). Via the serial port (RS232) of the PC and an XChecker™ cable, the XILINX™ configuration file is downloaded. Additional test equipment is controlled and read out via an IEEE 4888 interface and the general purpose interface bus (GPIB):

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[23] The company IMEC in Belgium (http:\\www.imec.be) co-ordinates the Europractice project.

- Pulse generator HP 81110A: 330 MHz, 2 channels, 2 ns rise time; used to inject charge into the CSA
- Logic Analyser HP 54645D: 16 digital channels, 2 analog channels; debugging of digital signals from/to XILINX™ and FIFO
- Oscilloscope HP 54825A: 4 analog channels, 500 MHz bandwidth, 2 GSamples/s, FFT[24]
- SourceMeter[25] Keithley 2400: Source voltage 5 µV...210 V, measure voltage 1 µV...211 V, source current 50 pA...1.05 A, measure current 10 pA...1.055 A); precise current measurement (e. g. subthreshold characteristics, DACs), high voltage power supply for silicon detector

Both the Blueboard and the dedicated PCB are powered by one power supply (AMREL LPS 304) with two separate outputs.

The Blueboard can accommodate additional daughter cards to provide not only a digital input/output connection but also analog information, i. e. special DAC-cards or ADC-cards to convert digital outputs to analog outputs or analog inputs to digital inputs respectively. Power cards can provide regulated supply voltages. Their voltages and currents can be monitored by the PC. SMUs (Source monitoring units) can replace external current sources and provide a constant current. The current or voltage is controlled and monitored by the computer. These daughter cards were used in the first version of the chip. Their functionality was more and more implemented in the chip itself in the later versions.

A photo of the setup in a Faraday cage is shown in Figure 5.2.

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[24] FFT: Fast Fourier Transform; to calculate frequency domain from time domain

[25] SourceMeter™: Combination of a precise, low-noise, highly stable DC power supply with a low-noise multimeter

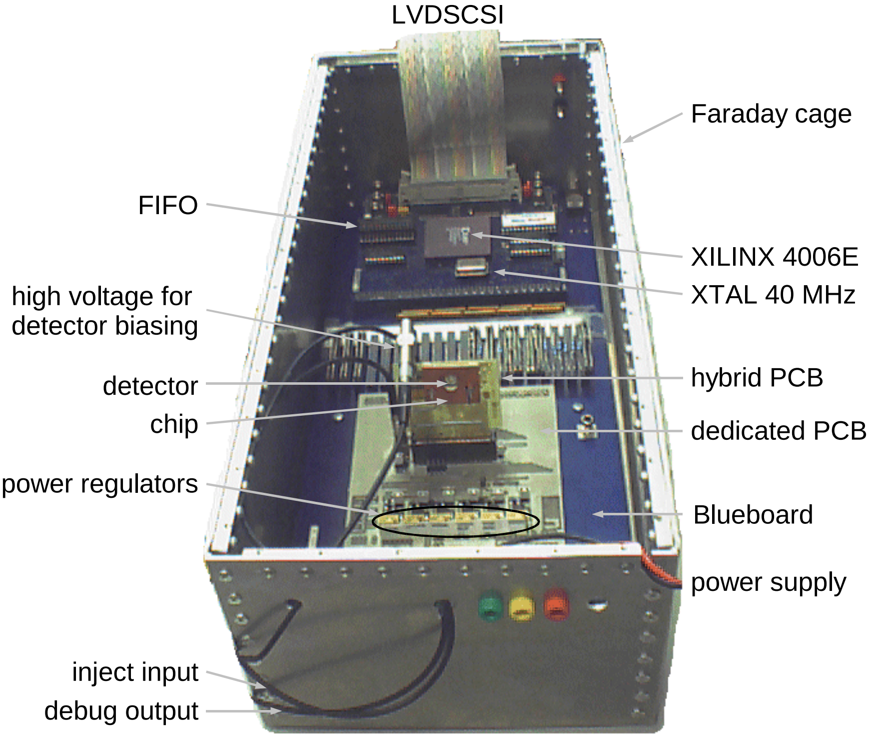

Figure 5.2 Photo of the Faraday cage housing the setup

5.1 Printed Circuit Boards

For each version of the chip a dedicated printed circuit board was developed. Each of them, except the test card for the first version, contains voltage regulators to provide stable voltages, which can be adjusted by high-precision multi-turn potentiometers (25 revolutions).

An overview of the different boards is given in Table 5.1.

<table>
<tr><td>chip</td><td>Ramses 1</td><td>Ramses 2</td><td colspan="2">Ramses 3</td></tr>
<tr><td>carrier</td><td colspan="3">JLCC84</td><td>hybrid
edge connector
RZB30DCHN</td></tr>
<tr><td>ADCs
(ADS 7818E)</td><td>0</td><td>2</td><td colspan="2">2</td></tr>
<tr><td>voltage regulators
(LM 317)</td><td>–</td><td>6</td><td colspan="2">6</td></tr>
<tr><td>resistors</td><td>30</td><td>11</td><td colspan="2">4</td></tr>
<tr><td>potentiometers</td><td>5</td><td>6</td><td colspan="2">7</td></tr>
<tr><td>capacitors</td><td>23</td><td>17</td><td colspan="2">14</td></tr>
<tr><td>LEMO jacks (I/O)</td><td>4/8
(inject, 2×CRRC, analog in; div. outputs)</td><td>1/2
(inject input; debug output)</td><td colspan="2">1/2
(inject input; analog output)</td></tr>
<tr><td>power supply</td><td>by power card from Blueboard</td><td colspan="3">two external (analog/digital)</td></tr>
<tr><td>power consumption without chip</td><td>–</td><td>96 mA</td><td colspan="2">38 mA for V≥8 V</td></tr>
</table>

Table 5.1 Overview of the dedicated printed circuit boards

The digital power supply voltage for the chip is kept low (typically less than 3 V) to avoid crosstalk of the digital circuitry to the analog signals, since the capacitive coupling is reduced with a lower amplitude of the digital signals and current spikes are reduced due to slower slew rates. Down to 2 V supply voltage, the digital output signals are correctly interpreted by the XILINX™. To limit the XILINX™ output signals (typ. up to 5 V) to the lower digital supply voltage, the protection diodes in the pads are misused. Serial resistors between the XILINX™-outputs and Ramses-inputs limit the currents. The resistances are a compromise between speed and low current. Typical values lie between 100 Ω and 4.7 kΩ.

Since the voltage regulators can only source current, but V_{CCA} needs sinking capability (current flows from V_{DDA} into V_{CCA}), an additional resistor between the regulator's output and ground is used to sink this current. The resistance is determined by considering the maximal sinking current and the power dissipation of the voltage regulator. From a worst case calculation (1000 pixels drawing 40 µA=40 mA; V_{CCA}=1.25 V) a resistance of 30 Ω for an array of 1000 pixels has to be used. For the test chip with 64 pixels even higher currents up to 200 µA per pixel can be sunk by the implemented resistor of 200 Ω. If no current has to be sunk, the voltage regulator has to source the total current into the resistance, which may not exceeds the maximum operating limits for the regulator (I_{max}=100 mA; P_{max}=2 W with heat sink).

For 'Ramses 3' a PCB for a hybrid board[26], on which the chip and detector is directly bonded, has been developed. A photo of this PCB is shown in Figure 5.3.

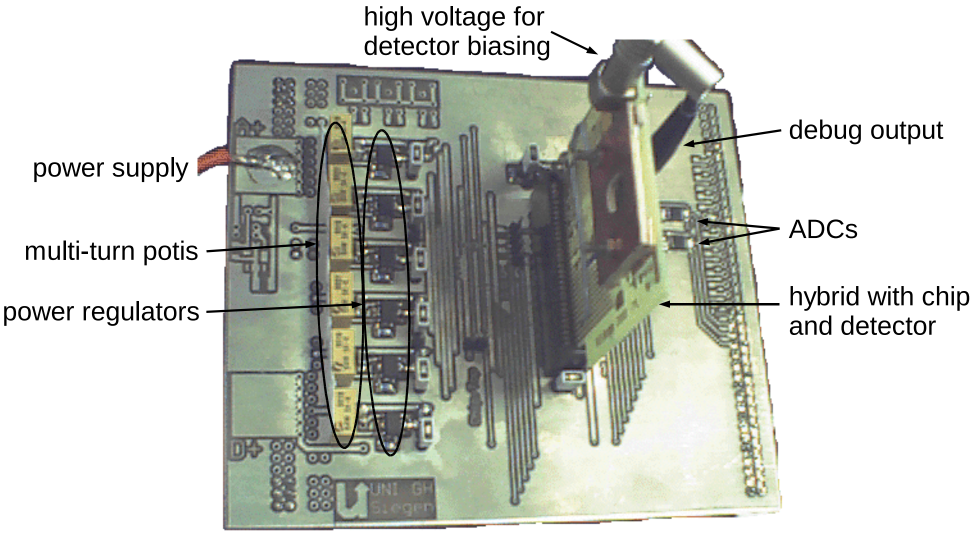

Figure 5.3 PCB with edge connector, into which the hybrid is plugged into

A photo of the gold-plated hybrid is shown in Figure 5.4.

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[26] The hybrid board was designed and kindly provided by M. Lindner, Physikalisches Institut - Universität Bonn.

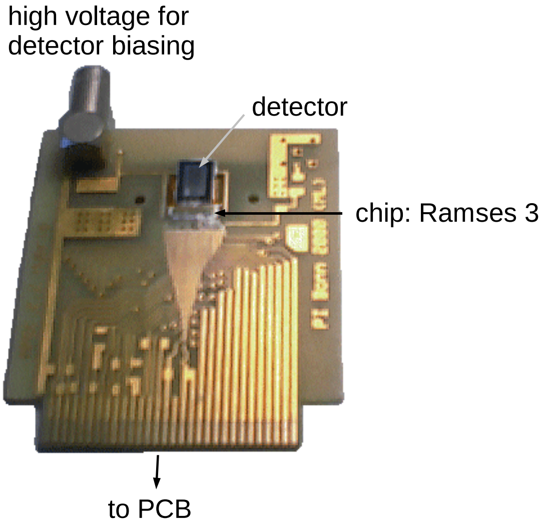


Figure 5.4 Detector and chip mounted on the hybrid

The smallest amplitude of the pulse generator is 100 mV. To apply even smaller pulses, a voltage divider is integrated on the PCB near the inject-input of the chip. A schematic of this divider is shown in Figure 5.5.

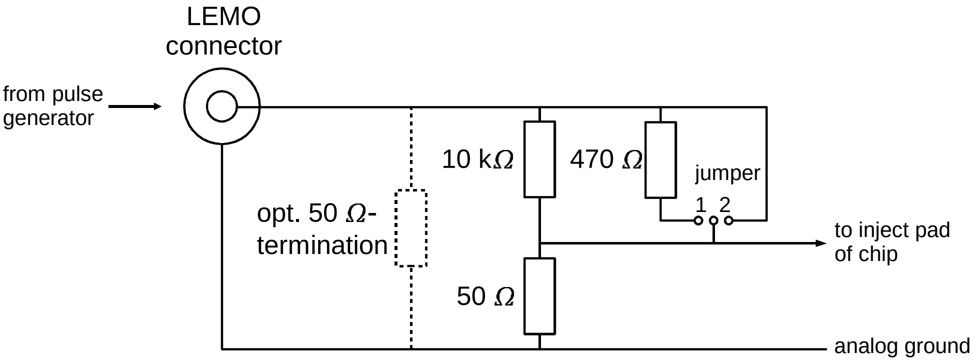
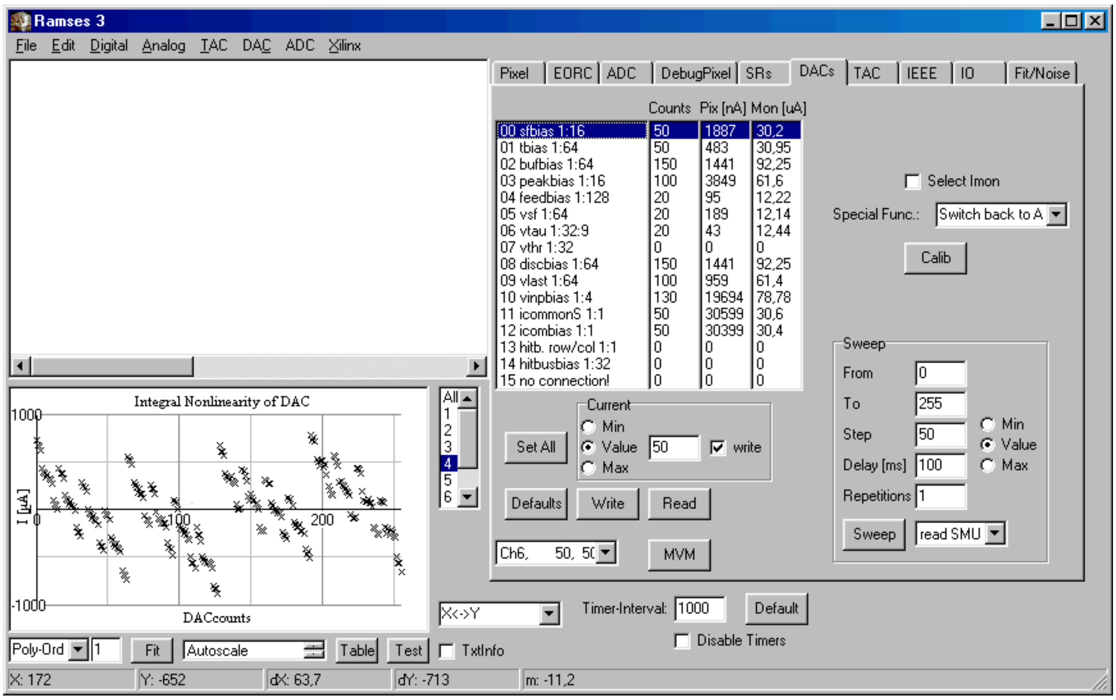


Figure 5.5 Voltage divider to scale down inject-signal

If the jumper is left open, then the 10 kΩ- and 50 Ω-resistor form a voltage divider, which scales the inject signal as 50/10050≈1/200. In position '2', the jumper directly shortens the 10 kΩ-resistor, connecting the LEMO connector to the inject pad (no voltage division). The 50 Ω-resistor automatically cares for a correct termination. If the jumper is set to position '1', the 470 Ω-resistor is connected in parallel with the 10 kΩ-resistor forming an effective resistor of 449 Ω. The voltage divider of this 449 Ω-resistor and the 50 Ω-resistor scales the signal as 50/499≈1/10. An optional 50 Ω-termination has also been foreseen on the board.

5.2 Test Software

To test the chips, a graphical software interface (Borland C++ Builder 4.0) for Windows 98 has been developed to communicate with the Blueboard and the GPIB-devices. The source code grew with the rising complexity of the chip to the considerable extent of nearly 15000 lines of source code. A screenshot of the program is shown in Figure 5.6.



	Counts	Pix [nA]	Mon [uA]
00 sfbias 1:16	50	1887	30,2
01 tbias 1:64	50	483	30,95
02 bufbias 1:64	150	1441	92,25
03 peakbias 1:16	100	3849	61,6
04 feedbias 1:128	20	95	12,22
05 vsf 1:64	20	189	12,14
06 vtau 1:32:9	20	43	12,44
07 vthr 1:32	0	0	0
08 discbias 1:64	150	1441	92,25
09 vlast 1:64	100	959	61,4
10 vinpbias 1:4	130	19694	78,78
11 icommonS 1:1	50	30599	30,6
12 icombias 1:1	50	30399	30,4
13 hitb. row/col 1:1	0	0	0
14 hitbusbias 1:32	0	0	0
15 no connection!	0	0	0

Current
○ Min
● Value 50 ☑ write
○ Max

Ch6, 50, 5(

☐ Select Imon
Special Func.: Switch back to A

Sweep
From 0
To 255
Step 50
Delay [ms] 100
Repetitions 1
○ Min
● Value
○ Max
read SMU

X<->Y
Timer-Interval: 1000
☐ Disable Timers

Poly-Ord 1
Autoscale
☐ TxtInfo

X: 172 | Y: -652 | dX: 63,7 | dY: -713 | m: -11,2

Figure 5.6 Screenshot of the dedicated test software

A short overview of some features of the software is given:

- Displays measurements and apply curve fits, both for analytical fits of polynomials and numerical least square fits for parameter estimation by means of the Levenberg-Marquardt algorithm.
- Testing of shift registers by generating various test patterns
- Loading DAC-values into the chip-registers
- Sets the channels to be monitored
- Load/Save default settings of individual chips
- Control of ADC-readout
- Display of hit-maps, threshold distributions and DC offsets of the whole pixel matrix
- Communicate via GPIB with various measuring instruments (oscilloscope, SourceMeters, logic analyser and pulse generator) to automate measurements
- Download XILINX™ bit-file via the parallel port and a proprietary cable

6 Performance/Measurements

This chapter presents the important measurements and the performance specifications of the three chip revisions. Also the measured spectrum of a Cd-source with a detector test structure will be presented.

The performance and measurements refer to the third version of the chip, unless stated differently.

6.1 Shift registers

Six shift registers are implemented: One shift register (select shift register, 8 bits) to select the clock distribution for the other five registers (see section 4.14.4).

The select shift register cannot be tested explicitly, because no extra output pad was spent for this purpose. Its correct functionality is concluded, if the other shift registers are proven to work well.

The shift registers are tested by applying random sequences and comparing the returning data with the applied sequence. A shift register is said to be working, if no difference between returning data and applied data occurs.

The shift registers work up to 200 kHz (typical clock generated by the software running on a 900 MHz computer) for V_{DDD}=1 V. For higher supply voltage, the maximal frequency increases. At V_{DDD}=2 V the maximal shift frequency is limited by 7 MHz. The upper limit for the clock frequency can be increased up to 11 MHz at V_{DDD}=6 V. The lower limit for the shift frequency (as the shift registers are only semi-static) is technology, temperature and illumination dependent[27] and typically below 0.1 Hz. The power consumption raises linear with clock frequency, because in CMOS logic significant current flows only during switching. The measured slope *(dI/dv)* of the current versus clock frequency at V_{DDD}=2 V is given in the last column of Table 6.1.

---

[27] The very small parasitic capacitors, which store the data within the shift registers, are discharged by leakage currents of transistors. All the physical effects responsible for higher leakage currents (e. g. higher temperature or energy deposition by photo effect) have an impact on the minimal shift frequency.

number of shift register	name of shift register	dI/dv [µA/kHz]
0	DACSR	60.2±0.1
1	IMUXSR	40.2±0.1
2	AnalogOutSR	42.8±0.1
5	PIXELSR	226.6±0.1
7	EORCSELSR	44.4±0.1

Table 6.1 Shift register number in the select shift register and current versus frequency characteristic of all shift registers

As the digital output of the chip drives the input of a XILINX™ (V_{DD}=5 V), the digital power supply is typically above 2 V to ensure logic-levels, which are correctly interpreted by the XILINX™.

6.2 Current Sources

6.2.1 Reference Current

The reference current is generated by the circuit in Figure 4.53. It is used in the reference voltage generator for the DACs, as shown in Figure 4.46. To measure the reference current, all DACs are set to 64 to mirror exactly the reference current. Each current can be externally measured between the monitoring pads (IMON) by adequate programming of the monitoring multiplexer. The 15 DAC currents vary between 37.5 µA and 40.0 µA, as shown below inFigure 6.6, with an average of I_{ref}=39.45±0.44 µA (V_{DDA}=4 V), as verified on three chips. According to the simulation, 50 µA were expected. To explain the deviation with a systematic increase in the resistor values due to process variation, a resistance 25 % larger than the design value of 2 kΩ, must be assumed, which exceeds the maximal process fluctuation of 15 %. Insistent investigation shows an incorrect simulation of the resistors. The resistor model for the AMS process is wrong. It extracts resistors for simulation, which are 16 % to small. A simulation with the hand-extracted resistors based on the process parameters results in a reference current of 41.27 µA, which is in quite good agreement ($<$ 5 %) with the measured value. The remaining deviation from the simulated value is in total agreement with the specified process parameter variation.

After an appropriate modification of the simulation, taking the higher resistances into account, the cascode voltages are compared to the measured values: The simulated lower cascode voltage (V_{cascN}) is 1.48 V, the measured value 1.54 V. These values are in good agreement and the deviation has no consequences for other blocks. The higher cascode voltage (V_{cascP}), which is generated by the reference current flowing through a diode connected transistor in series with a resistor (12 kΩ), is simulated to be 1.77 V below V_{DDA}. The measured value of 1.68 V below V_{DDA} is also in pretty good agreement with the simulated value.

The supply voltage dependence of the reference current is plotted in Figure 6.1. By taking the difference of the current into V_{DDA} between all DACs off and DAC 15 set to 64 (increase in total current by the reference current), the reference current is determined. From this measurement the voltage range, in which the reference circuit works, is extracted: The reference current I_{ref}=39.33±0.18 µA for 2.3 V≤V_{DDA}≤5 V for this chip. In this voltage range the power supply sensitivity ($\Delta I_{ref}/I_{ref}$:$\Delta V_{DDA}/V_{DDA}$) is approximately 0.02 (10 % change in power supply causes a 0.2 % change in reference current). The lower limit of the power supply voltage is in good agreement with the simulated value of 2.25 V.

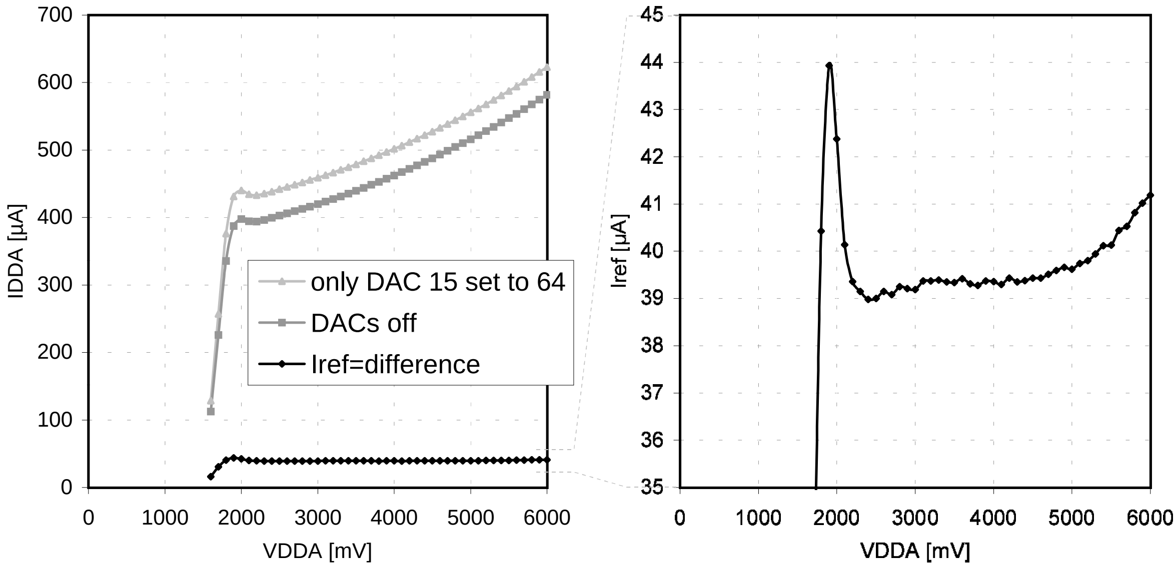


Figure 6.1 Measurement of the current into V_{DDA} to determine the voltage dependence of I_{ref}

The chip was designed to work with V_{DDA}=4 V. The process specific maximal ratings without degradation[28] limits the supply voltage to maximal 5.5 V.

Another important characteristic of a DAC is its output resistance. An ideal current source has an infinite output resistance, i. e. the current is independent of the output voltage. To measure the output characteristic, the output voltage is swept over the supply voltage range (here V_{DDA}=4 V). The output current versus output voltage is shown in Figure 6.2.

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[28] For quick measurements an maximal exposure to V_{DDA}=7 V is allowed.

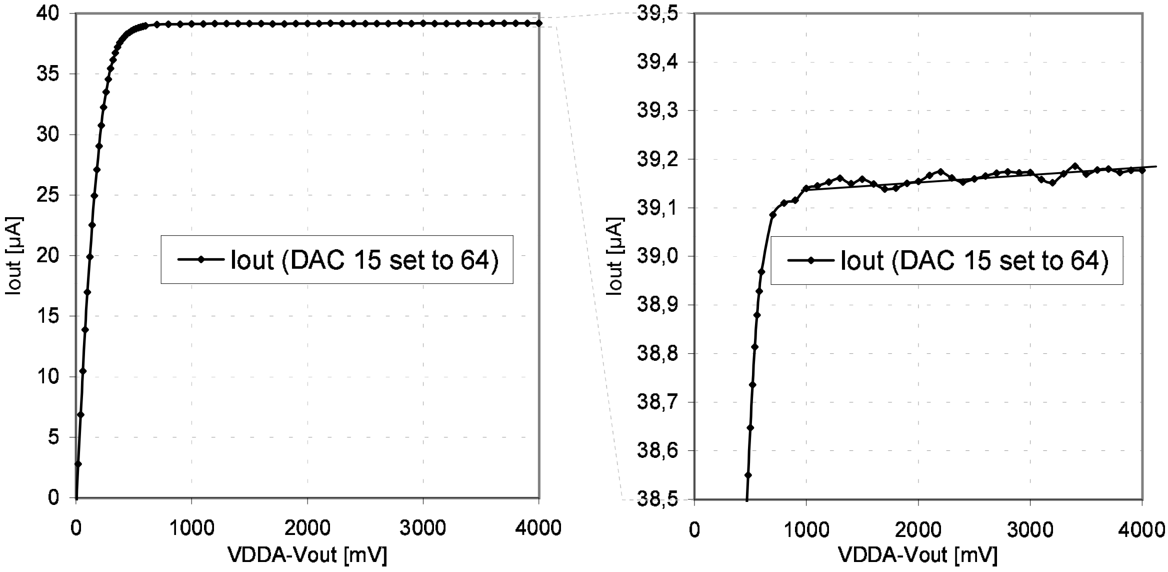

Figure 6.2 Output characteristic of the DAC

The output voltage is given with respect to V_{DDA}, because the cascoded output current mirror consists of PMOS transistors as shown in Figure 4.47. For an output voltage above 700 mV the output current is within 1/20 of a LSB, which is extremely good. From a linear fit an output resistance of $R = \partial V_{out} / \partial I_{out} \approx 60\ \mathrm{M}\Omega$ is extracted.

To determine the temperature dependence of the reference current, the temperature was measured with a K-type temperature sensor and a multimeter (Voltcraft® M−3860M). The relation and a linear approximation is shown in Figure 6.3.

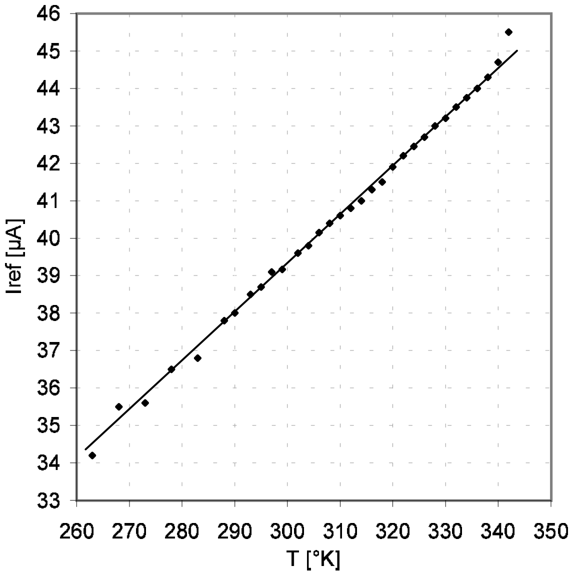

Figure 6.3 Reference current versus temperature

From the extraction of the best fit, the zero is found to be $T(I_{ref}=0\ \mu\text{A})=0.2$ °K. Using the slope (131 nA/°K) and equation 4.51, nk/qR is determined:

$$\frac{nk}{qR}=\frac{\Delta I}{\Delta T}\cdot\frac{1}{\ln 8}=63\,\text{nA/K} \;\Rightarrow\; n=1.50 \tag{6.1}$$

The emission coefficient $n=1.50$ is consistent with the simulated value of $n=1.48$. It should not be hidden that the temperature coefficient of the resistor $(0.75\cdot 10^{-3}/\text{K})$ has not be considered in this analysis. In the range from $T=260...340$ °K the resistance varies by 3 % of the nominal value ($R(T=300\ \text{°K})=2.06\ \text{k}\Omega$).

6.2.2 Digital-to-Analog Converters

To investigate the linearity of the DACs, the current dependence on the digital code is measured. A representative plot is given in Figure 6.4.

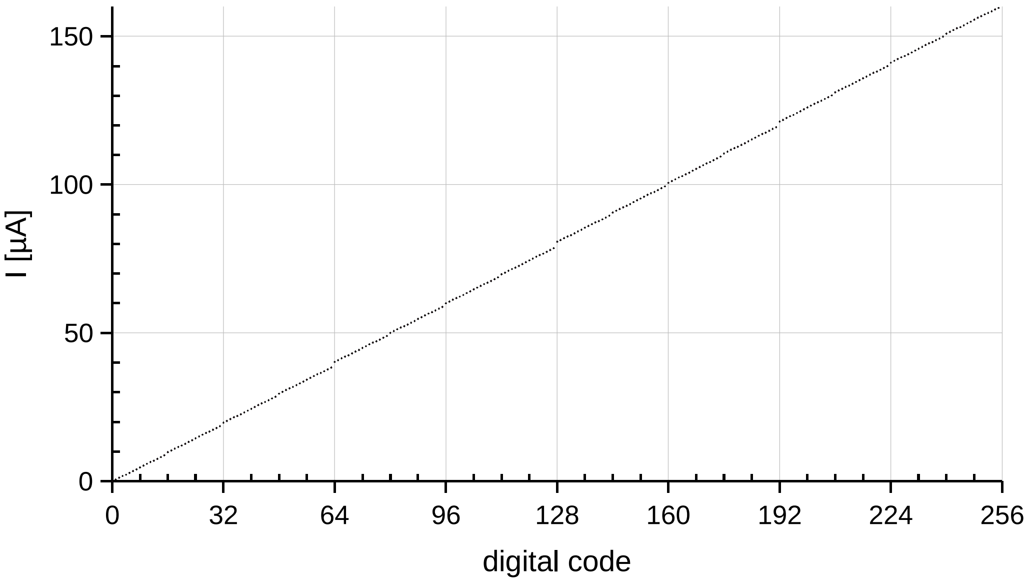

Figure 6.4 DAC-output current versus digital code

At first sight, the current shows a good linear correlation to the digital code. To investigate the linearity more quantitative, the deviation from the best linear fit is plotted in Figure 6.4.

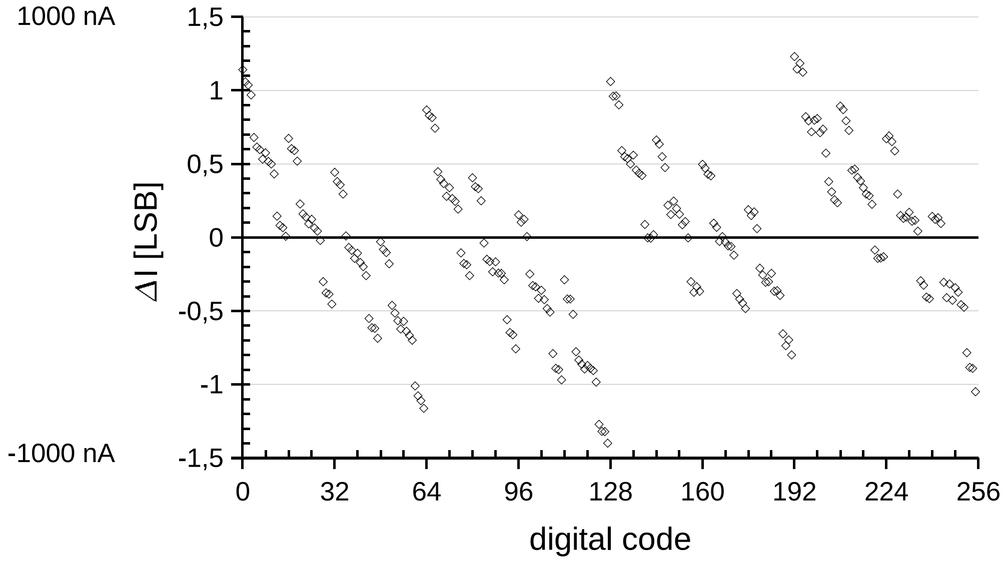

Figure 6.5 Non-linearity of the DAC

The maximal deviation from the best fit is referred to as integral non-linearity (INL), the maximal difference of two successive codes is referred to as differential non-linearity (DNL). Both values are used to specify the linearity of a DAC. The implemented DAC shows an INL=1.5 LSBs (least significant bits) and a DNL=2.5 LSBs (code 127 to code 128), which is relatively large compared to commercially available DACs, but sufficient for the present application. In spite of the large DNL, the DAC is still monotone. This means that an increase in the digital code always results in a higher output current.

All fifteen DACs have been tested and work sufficiently well. To get an idea of the output current spread due to threshold voltage variation, the reference current (DAC set to 64) for all DACs is plotted in Figure 6.6.

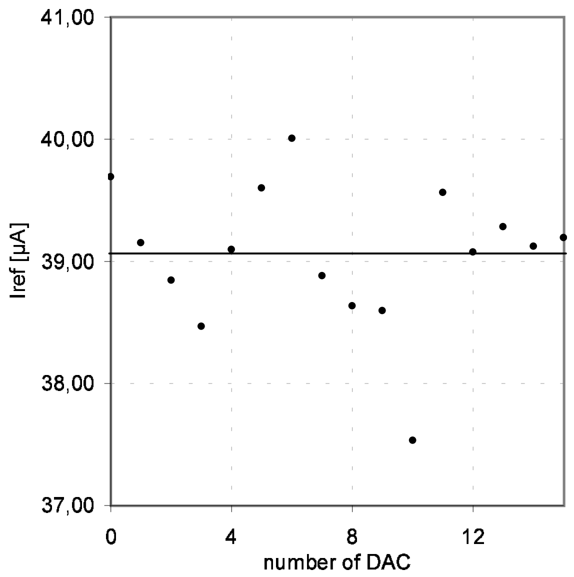

Figure 6.6 Output current spread for all DACs due to threshold voltage variation

The deviation of the measured currents from the mean current of 39.05 µA (solid line) amounts σ=0.58 µA (1.5 %).

Assuming that the spread is caused by threshold voltage variation in the output current mirror of the DAC, the threshold voltage variation is calculated according to equation 8.30:

$$\Delta V_{thr} = \frac{0.58\,\mu\mathrm{A}}{2\cdot 39.05\,\mu\mathrm{A}}(V_{GS} - V_{thr}) = 0.74\,\%\sqrt{\frac{2I}{\beta}} = 1.7\,\mathrm{mV} \tag{6.2}$$

The dimensions of the output transistors to calculate β are $W/L = 4\cdot 18/2$.

Moreover, considering that the output current is formed by a 4:4 mirror to counteract threshold variation, the local spread is calculated to be

$$\Delta V_{thr} = 1.7\,\mathrm{mV}\cdot\sqrt{4} = 3.4\,\mathrm{mV} \tag{6.3}$$

The maximal threshold voltage variation is specified as ±100 mV for long channel devices[29]. Assuming a flat distribution implies σ_{thr}=58 mV. The local, relative threshold variation is noticeable lower than the absolute specified chip-to-chip spread or an on-chip variation.

---

[29] The maximal threshold voltage variation for short channel devices is specified within ±120 mV.

6.3 I/O-Pads

6.3.1 Digital Input Buffer

The functionality of the protection diodes in the schematic of Figure 4.57 are measured by varying the input voltage from −1 V to V_{DDD}+1 V. The characteristic for V_{DDD}=V_{DDDBUF}=3.0 V is shown in Figure 6.7.

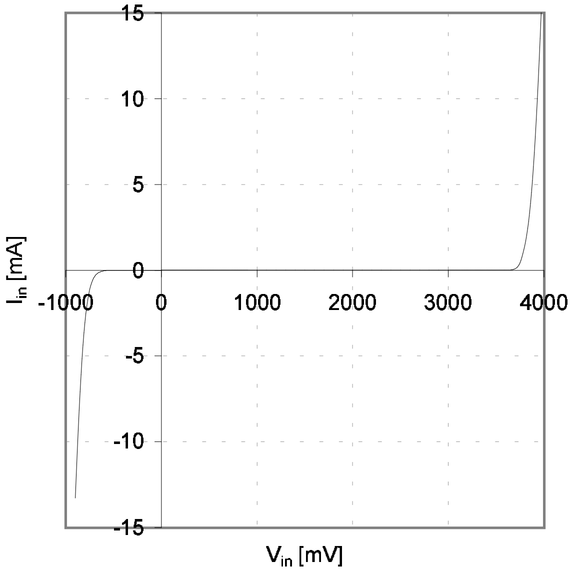

Figure 6.7 Functionality of the protection diodes

If the input voltage exceeds the power supply limits by at least 0.6 V, the protection diodes starts conducting. The input characteristic over the regular input range is shown in Figure 6.8.

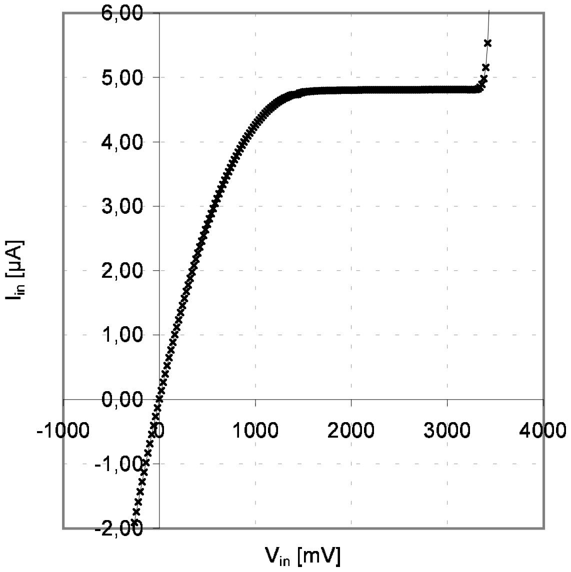

Figure 6.8 Input current over the regular input voltage range with pull down characteristic

The shown input pad has pull down characteristic: If no voltage is applied, the input voltage is tied to ground by an effective resistance of 150 kΩ (transistor in linear region, see section 4.14.2). For a higher input voltage the input current saturates at 4.8 µA (for V_{DDD}=3 V). The effective resistance is supply voltage dependent as shown in Figure 6.9.

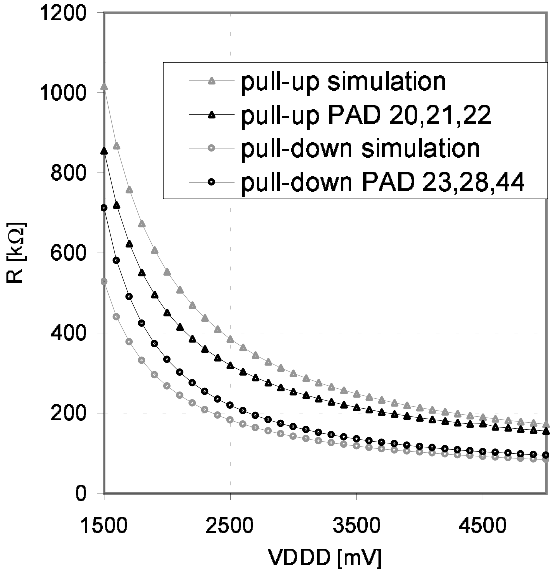

Figure 6.9 Effective input resistance versus supply voltage

The simulated resistances for the pull-down pads are lower than the measured values for all three pull-down pads, which are consistent among each other. The simulated resistances for the pull-up pads are higher than the measured values for all three pull-up pads. The deviation between the measured and simulated resistances does not derogate the functionality of the chip and seems to be a deficit of the model for the fairly long channel devices (L=22.8 µm).

6.3.2 Digital Output Buffer

The output resistances of the output buffer is measured for $V_{DDD}=V_{DDDBUF}$=3.0 V by applying two different external voltages and measuring the current difference[30] ($R_{out}=\Delta U_{out}/\Delta I_{out}$). Table 6.2 shows the measured DC-resistances and the simulated values.

logical output state	R$_{out}$ [Ω]	
	measured	simulated
low	40	33
high	62	54

Table 6.2 Output resistances

The deviation between the measured and simulated values can be explained by an additional serial resistor (≈7 Ω), formed by wire bonds, sheet resistances of metal layer inside the chip and wiring resistances on the PCB. A low output resistance is required for high speed. The rise time and fall time respectively, of the output into an oscilloscope probe (10 MΩ || 9 pF + additional stray capacitances) are summarised in Table 6.3. The output resistance is extracted from the rise time or fall time respectively:

$$R=\frac{\tau}{C}=\frac{\Delta t}{C\ln 9}=\frac{\Delta t}{2.2C} \tag{6.4}$$

Δt has to be substituted by the corresponding rise time or fall time.

load [nF]	rise time [ns]	R_{out} [Ω]	fall time [ns]	R_{out} [Ω]
0.018	2.60 ± 0.18	66 ± 5	1.51 ± 0.23	38 ± 6
50	6417 ± 202	58.3 ± 1.8	4596 ± 65	41.8 ± 0.6
100	13130 ± 230	59.7 ± 1.1	9536 ± 170	43.3 ± 0.8
200	26310 ± 377	59.8 ± 0.9	19493 ± 304	44.3 ± 0.7

Table 6.3 Rise time and fall time for different loads; resulting output resistances

Both methods show good agreement for the output resistances.

---

[30] Alternatively a current can be provided and the voltage drop (to V_{DDD} or GND respectively) can be measured.

6.3.3 Analog Output Buffer

In order to correctly interpret the analog information, which is buffered by the analog pad, the latter has to be characterised. Therefore the inject-input line is misused, which can be routed to the output buffer via the output multiplexer as shown in Figure 6.10.

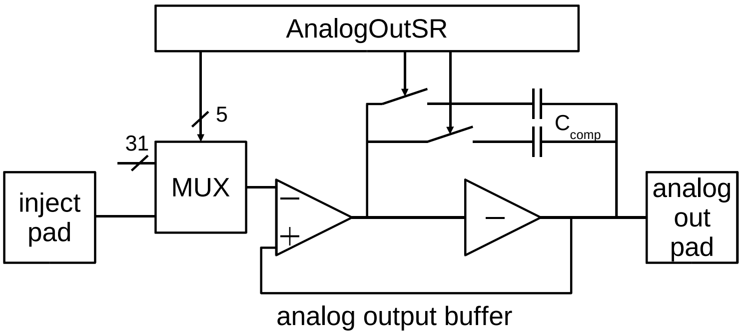

Figure 6.10 Internal setup to measure analog output buffer

The output buffer offers the possibility to route two compensation capacitors in the output buffer stage. Three different states (two bits) define the value of the feedback capacitor as listed in Table 6.4.

shift register value binary (decimal)	C_{comp} [fF]	comment
00 (0)	1000	full compensation, lowest slew rate; short settling time
01 (1)	500	moderate compensation, slew rate and settling time
10 (2)		
11 (3)	0	no compensation, fastest slew rate; long settling time

Table 6.4 Values of the compensation capacitors

The larger the compensation, the lower the slew rate[31] and the shorter the settling time[32]. Depending on the requirements, the optimum can be adjusted. The maximum compensation is used as default setting. Another impact on slew rate is given by the DAC settings (DAC 11, 12). The larger their bias current, the faster the slew rate. Usually both DACs are set to the same value of 50 counts (30 µA). The effect of different compensation capacitors and DAC values is shown in Figure 6.11. To clarify the effect, a relatively large load capacitance of 230 pF (2 m coaxial cable (200 pF) to oscilloscope (10 pF) in parallel with the input of the ADC (15 pF)) is used. The supply voltage V_{DDABUF}=4.0 V.

---

[31] slew rate [Hor 89]: maximum slope of the signal [V/s]

[32] settling time [Hor 89]: time required to get within some specified amount of the final value

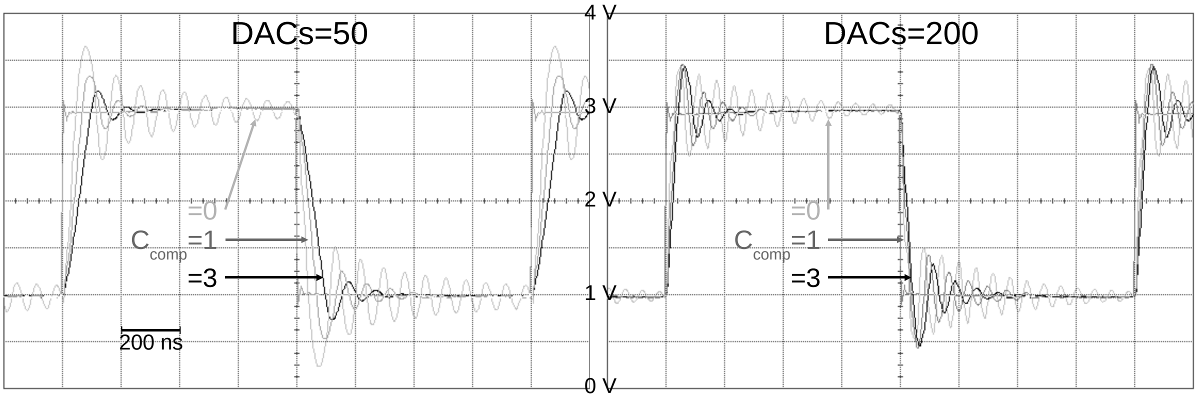

Figure 6.11 Response of the analog output pad for different DAC settings and compensation capacitors

For the default setting (DACs=50, C_{comp}=max) and a more realistic load of 30 pF the response to a voltage step from 1 V to 3 V is shown in Figure 6.12.

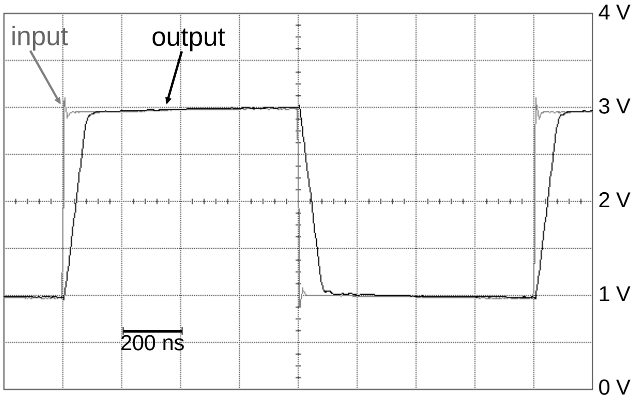

Figure 6.12 Response of the analog buffer for a realistic load of 30 pF||10 MΩ; DACs=50, C_{comp}=1 pF

The slew rate and settling time for different load capacitors, DAC settings and compensation capacitors are summarised in Table 6.5.

For the low capacitive load the settling time for a compensation capacitor of 1 pF is with 150 ns (DACs=50) sufficient fast for a readout cycle below 1 MHz. The maximum sampling rate of the subsequent ADC is 500 kHz, the acquisition time 350 ns. It should be mentioned that an even higher slew rate is achieved by a higher supply voltage of the analog output pads.

		slew rate [V/µs]			settling time within 1 % of the final value [µs]		
load [pF]	DAC	C_{comp}=0	C_{comp}=1	C_{comp}=3	C_{comp}=0	C_{comp}=1	C_{comp}=3
230	50 (30 µA)	23	35	54	0.4	0.45	1.6
	200 (120 µA)	52	58	73	0.4	0.45	1.4
30	50 (30 µA)	26	45	113	0.15	0.23	0.5
	200 (120 µA)	81	112	164	0.53	0.53	0.53

Table 6.5 Slew rate and settling time of analog output

In Figure 6.13 the offset voltage $(V_{offset}=V_{out}-V_{in})$ of the analog output buffer is shown for different input voltages. It shows that the output buffer operates over the full supply voltage range (rail-to-rail), although the error due to the voltage offset grows as the input voltage sweeps towards the supply borders.

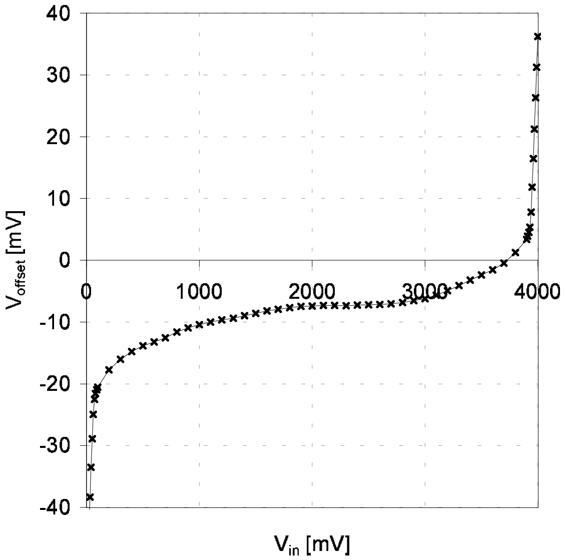

Figure 6.13 Offset voltage of analog output buffer

The bandwidth is measured by sweeping the frequency of a sine-signal and measuring the ratio between input and output signal. The point, at which the ratio drifts from unity, is defined as the bandwidth. It is measured to be about 5...6 MHz in the output voltage range 0.5...$V_{DDABUF}-0.5$ and about 1 MHz for the full output voltage range.

By means of the analog output buffer the voltage divider on the printed circuit board is tested. Figure 6.14 shows the response of the analog buffer to an inject-pulse, which is scaled down by a factor of 10 by the voltage divider implemented on the PCB. Distortion of the vertical frequency (76.5 kHz≙13.07 µs) of the nearby monitor are shown in light grey, which instantaneously vanishes, when the monitor is switched off (shown in black).

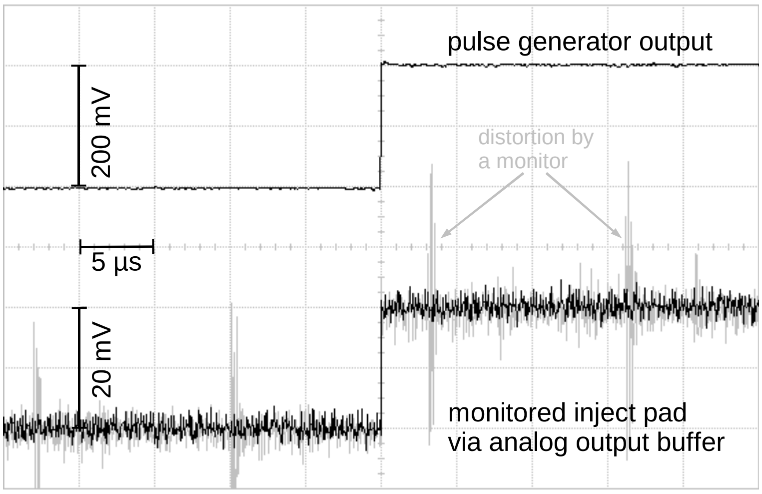

Figure 6.14 Monitoring the scaled (1:10) inject input signal

To test the 1:200-divider of the PCB, a 2 V signal is applied and monitored. The result is shown in Figure 6.15.

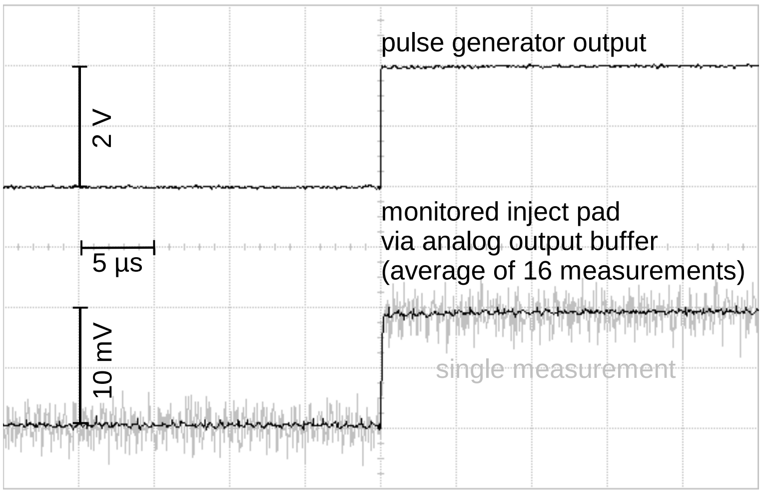

Figure 6.15 Use of the 1:200 voltage divider

By averaging 16 measurements (black curve) the noise is reduced and the absolute voltage swing of 9.5 mV can be determined. A single measurement is shown as a grey curve. The ratio of 9.5/2000=1/210 differs slightly from the designed value of 1/200 due to the additional load of the chip.

Although a Faraday cage (see Figure 5.2) is used for low noise measurements, beside the 76.5 kHz signal of the monitor several other interfering noise frequencies are determined, which are listed in Table 6.6.

Frequency	Source	Prevention
50 Hz/100 Hz	neon ceiling lamps, optical coupling via detector	covering of the set up by a black blanket
15.8 kHz	vertical frequency of liquid crystal display of oscilloscope	avoiding cables nearby the LCD, improved grounding scheme
125 kHz and multiples	phase lock loop (PLL) of the pulse generator	distance
5 MHz	SourceMeter (probably ADC)	additional blocking capacitors at the I/O of the SourceMeter
40 MHz and whole-numbered fractions	crystal oscillator on Blueboard (clock for ADCs)	plug off as long as no ADC is needed
100 MHz	oscilloscope	distance

Table 6.6 Origin of different noise frequencies

6.4 Pixel Performance

6.4.1 Charge Sensitive Amplifier

Ramses 1

The first version of the chip was submitted to verify the theoretical noise performance. A CSA similar to Figure 4.5 was implemented with small modifications:

- The CSA was designed for a (150 µm)^2 pixel in a 0.8-µm technology. The corresponding input transistor was wider than in Ramses 3; the bump bond pad was relatively small (15 µm diameter).
- A straight cascode was used instead of a regulated cascode ($T_{regcasc}$ omitted).
- The feedback reset consists of a single transistor operated in weak inversion. The gate voltage was externally supplied.

To determine the noise, several identical electrical test pulses are applied, while measuring the mean shaper output response and its deviation.

An electrical test pulse (4V/190) via a 10 fF capacitor generates $n{=}CU/q{=}1318$ e. The feedback capacitor was designed to be 2 fF. The mean output voltage (after shaper and output buffer) was 26.05 mV as shown in Figure 6.16.

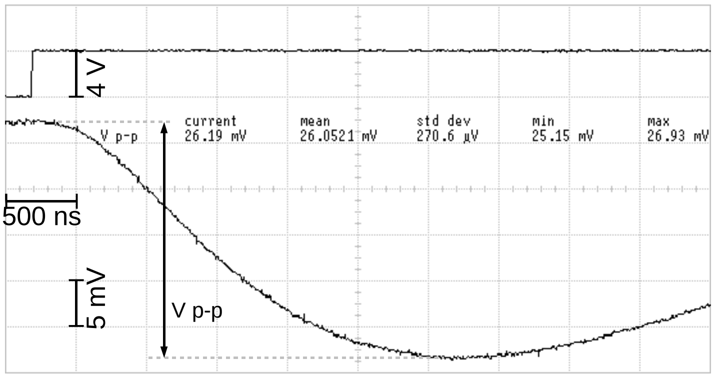

Figure 6.16 Determination of noise by measuring the peak-to-peak voltage of the shaper response to an injected charge

The noise corresponds to a deviation of the output signal around the mean value of 0.27 mV, which translates to a noise of

$$ENC_t = \frac{0.27\,\mathrm{mV}}{26.05\,\mathrm{mV}} \cdot 1318\,e = 13.7\,e \tag{6.5}$$

without detector (no leakage current noise), which is significantly larger than the expected noise of 9.1 e. The expected noise is calculated without considering the influence of the feedback mechanism[33] and noise contributions of the shaper and

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[33] As pointed out in section 4.2.3 the feedback noise contribution of a transistor operated in weak inversion is approximately the same as the detector leakage current noise.

subsequent electronic[34]. The test pulses and the resistive voltage divider contribute additional noise as well.

To investigate the dominant noise contribution, the total noise versus the input transistor bias current I_{input} is measured as shown in Figure 6.17.

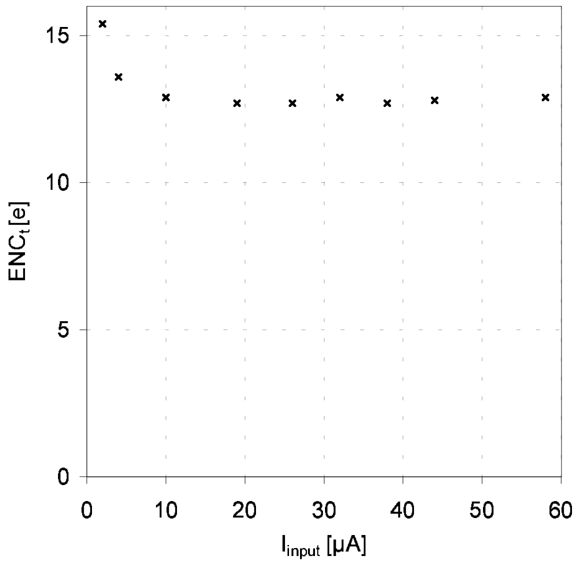

Figure 6.17 Total noise versus input transistor bias

If the dominant contribution to the total noise would be due to thermal noise, then a decrease in total noise with increasing biasing (lower channel resistance) were expected (g_m in equation 4.11 increases). This is seen for bias currents below 10 µA. As no detector is connected (no detector leakage current noise), the dominant contribution is assumed to be flicker noise. The flicker noise contribution is independent of the shaping time (equation 4.16). The total noise versus shaping time is shown in Figure 6.18.

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[34] According to [Cha 97] the input stage contributes 95 % to the overall noise.

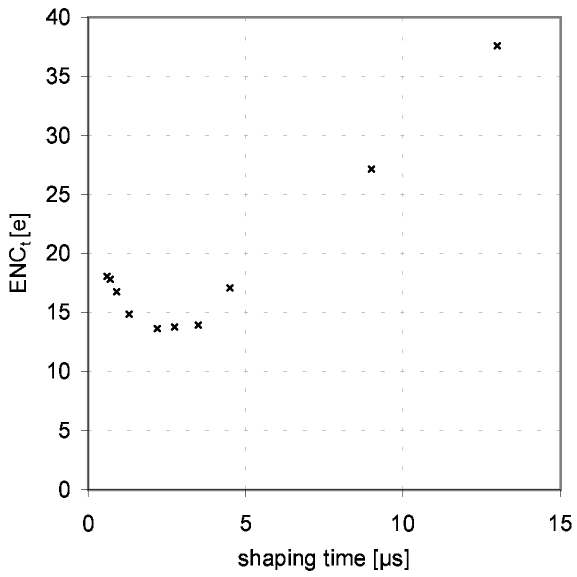

Figure 6.18 Total noise versus shaping time

The total noise should decrease with an increasing shaping time, which is true for shaping times below 4 µs. An increase can only be explained by a leakage current (see equation 4.19). The leakage current is extracted from Figure 6.18 in two different ways: From the optimal shaping time (lowest noise) and from the slope for large shaping times respectively.

According to equation 4.46, the leakage current I_o is calculated by using the optimal shaping time $\tau_{\mathrm{opt}}=2.65$ µs, which is extracted from a quadratic fit to the data around the minimum in Figure 6.18. The transconductance of the input transistor, biased at 20 µA, is $g_m=550$ µS. The total capacitance C_t (without detector) is estimated to $C_t=300$ fF.

$$I_o=\left(\frac{C_t}{\tau_{opt}}\right)^2\frac{k\,T}{q}\frac{4}{3\,g_m}=\left(\frac{300\,\mathrm{fF}}{2.65\,\mu s}\right)^2\cdot 25\,\mathrm{mV}\cdot\frac{4}{3\cdot 550\,\mu\mathrm{S}}=0.8\,\mathrm{pA} \tag{6.6}$$

Assuming that for large shaping times the leakage current noise is dominating *($ENC_t \approx ENC_o$)*, the leakage current can be determined from the slope of ENC_t^2 versus τ by using equation 4.44:

$$I_o=\frac{q}{1.85}\frac{\partial ENC_t^2}{\partial\tau}=0.86\cdot 10^{-19}\,\mathrm{C}\cdot 116\,\mu\mathrm{s}^{-1}\approx 10\,\mathrm{pA} \tag{6.7}$$

Comparing both currents to typical leakage currents (see sections 6.4.3 and 6.4.6) in the order of 10 fA, the first method seems to be more trustworthy.

The leakage current is probably generated by the leakage current of the reversed biased diodes of the feedback transistor.

The promising low noise measurements led to a further revision of the chip, integrating several features as DACs, reference circuits, a TVC, a complete matrix of 1024 pixels and an individual adjustable feedback in each pixel.

Ramses 2

The main step to Ramses 2 was a new and smaller technology (AMS 0.6 µm). The complete electronic has to be simulated once more and a complete layout was done. A TVC is implemented in each pixel and the dimension of the pixel is shrunken to (100 µm)^2. The gate voltage of the feedback transistor is adjusted by a global value, which is corrected by a two bit DAC in each pixel. Measurements show that the amplifiers tend to oscillate and that the feedback adjustments are insufficient to compensate for threshold variation. Bump bonding of a detector onto single chips turned out to be very difficult due to the small bump bond pad. A third version should extinguish all these deficits.

Ramses 3

To suit to existing detectors for gold stud[35] bonding, the bump bond pad is enlarged (Ø=45 µm) and the pixel size is matched to the detector pixel size (200 µm)^2. The additional free pixel area is used to implement additional debugging circuits, i. e. four unity gain buffers to monitor the CSA output, the shaper output, the peak detector and the voltage across the TVC-capacitor.

The most important improvement of the CSA in the third version is its auto-adaptive reset mechanism (see section 4.2.3). It turns out that the leakage current of the reverse biased bulk-source diode is lower than simulated and lower than the drain-source leakage current, therefore not able to raise the CSA input to the operating point – no test pulses could have been applied. To perform an electrical test, a detector with test structures (rectangular pixels with approximately 50 µm × 450 µm) is put beneath (instead on top of) the electronic chip and is bonded by wires. The wire-bonding is a challenge as the detector was foreseen to be bump bonded. Bump bond pads are significant smaller than wire bond pads and therefore more difficult to bond. A microscopic view of the proportions is shown in Figure 6.19.

The small detector bond pads (Ø≈12 µm) are difficult to hit with the significant larger wire. An uncertainty due to the mechanically positioning of the wire leads to further contacting problems. For comparison the relatively large wire bond pads are also shown in the figure on the right hand side.

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[35] gold stud bonding: A thermosonic gold wire bonder is used to place gold balls on the semiconductor bump pads. For assembly the die is inverted and dipped into a thin layer of silver filled epoxy. The die is then aligned and placed on the detector.

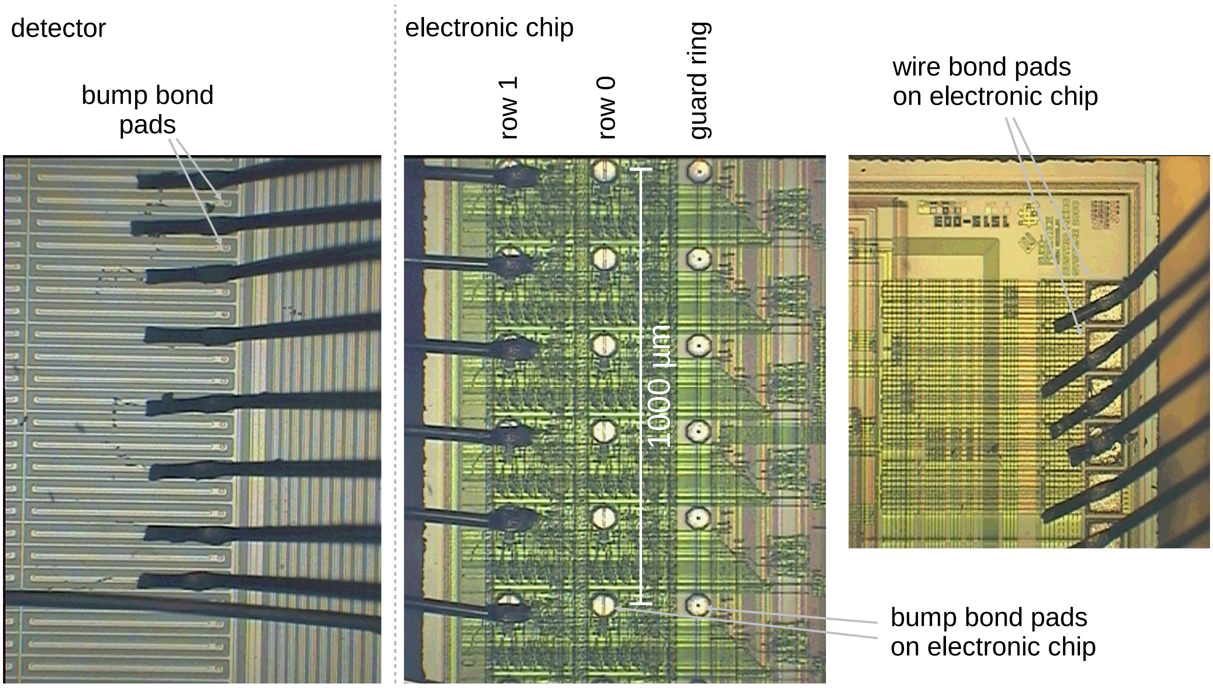

Figure 6.19 Detailed overview of the bonding challenge (from left to right): a test detector with rectangular pixels for bump bonding, the electronic chip with bump bond pads for gold stud bonding, the wire bond pads to connect the chip to the hybrid (to scale)

Eight of the bonded pixels could be verified to have a conductive connection to the electronic chip, two pixels are connected to large test diodes and two pixels are connected to the guard ring pads, which are connected to a wire bond pad to investigate the DC-characteristic of the feedback of these two pixels.

Feedback

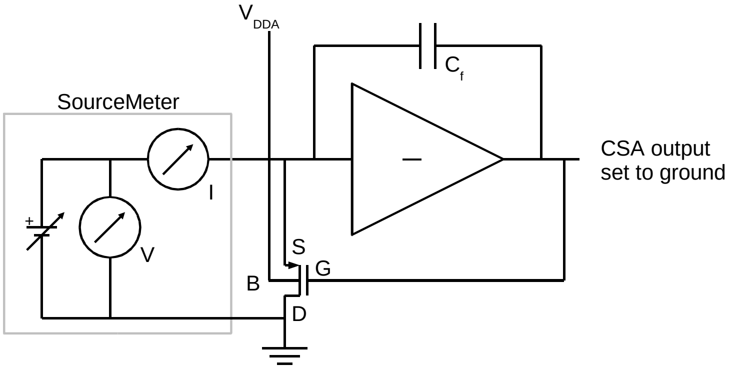

Figure 6.20 Setup for measuring the characteristic of the feedback transistor

With adequate DAC settings the CSA-output (gate voltage of the feedback transistor) is set to ground. The characteristic of the feedback PMOS-transistor can be measured since the input voltage refers to the gate-source voltage as shown in Figure 6.20.

The characteristic is shown in Figure 6.21. To extract the threshold voltage and the range of strong inversion, the square root of the current is plotted versus the input voltage. The threshold voltage is determined from the linear extrapolation: $V_{thr}(I=0\ \mu\mathrm{A})=1370$ mV (this higher threshold than specified is expected due to body effect, since bulk and source are not connected). A logarithmic plot of the intended subthreshold region and the simulation results are shown in the right hand plot.

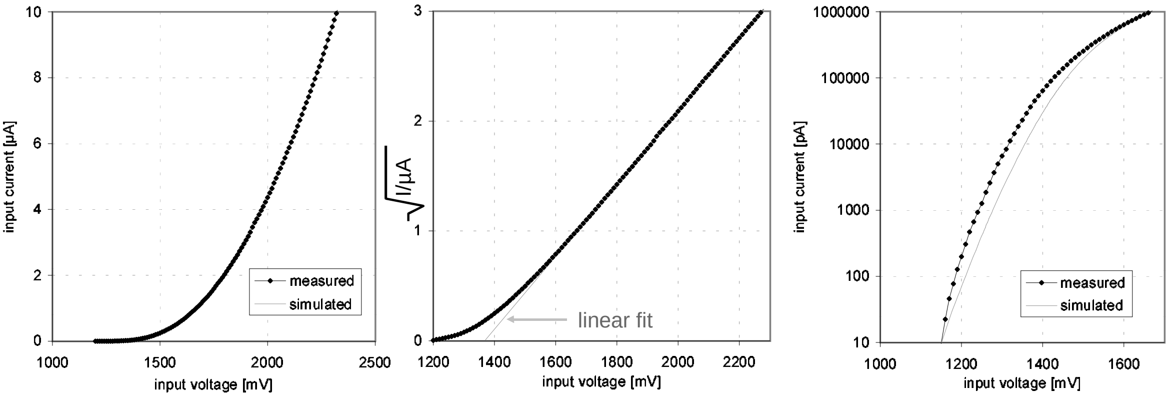

Figure 6.21 Characteristic of the feedback transistor

In strong inversion the measured characteristic is in excellent agreement with the simulation. In moderate and weak inversion a small, acceptable deviation is observed. The detector leakage current sets the operating point. The slope $(=q/nkT)$ of a linear fit in the logarithmic plot gives an emission coefficient of $n\approx0.5$ $(T=300\ \mathrm{K})$ for a typical current of 40 pA.

In the simulation the feedback mechanism worked well, i. e. the leakage current of the reverse biased diodes (bulk-source junction) is sufficient large to bring the CSA input to its operating point (about one threshold voltage below V_{DDA}). In reality the source-drain leakage current exceeds the bulk-source leakage current, therefore the operating point is not reached. The leakage current paths are shown in Figure 6.22.

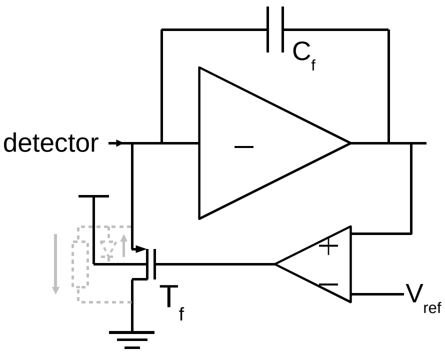

Figure 6.22 Leakage currents through the feedback transistor

The (larger) leakage current of the detector is needed for operation – test structures of a detector were therefore wire-bonded to the chip. Three[36] of the eight pixels, which are bonded to the detector, could be tested by applying both electrical test pulses and optical pulses.

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[36] Pixel 12, 15, 16 of the upper row can be tested

To calibrate the CSA, the inject capacitance has to be extracted. Figure 6.23 shows a cross section of the bump bond pad, which is also used as inject capacitor.

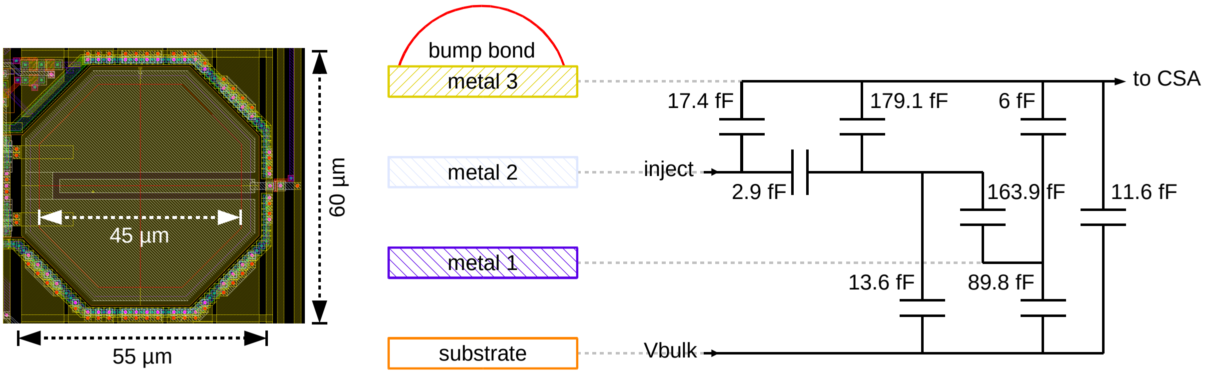

Figure 6.23 Layout and cross section of the bump bond pad to extract effective inject capacitance

The top level 'metal 3'-layer is used to form the bump bond pad, which is directly connected to the charge sensitive amplifier. The underneath placed 'metal 2'-layer forms an inject capacitor together with the pad itself. All other parasitic capacitances are also shown in Figure 6.23. Calculating the capacitance of the bump bond pad to the substrate regarding all parasitic capacitances yields approximately 63 fF. The effective inject capacitor is approximately C_{inj}=19.5 fF. If a voltage step is applied on the inject capacitor, an equivalent charge of $Q=C_{inj}\cdot U$ is deposited on the input of the CSA. A 50 mV voltage step translates to $n=C_{inj}\cdot U/e$=19.5 fF $\cdot$ 50 mV/1.6 $\cdot\, 10^{-19}$ C=6094 e.

Applying an inject signal of 50 mV (while the capacitive divider of Figure 4.8 b) is switched off by bypassing C_2) results in a voltage amplification A=19.5 fF/2 fF=9.75, if the designed value of the feedback capacitor C_f=2 fF is taken for granted. Figure 6.24 shows the response of the CSA for both cases: C_2 is bypassed or not. The measured value of 570 mV is 11.4 times larger than the 50 mV input signal, which is explained by a deviation[37] of the extremely small capacitors from the extracted values and the uncertainty in the reproducibility of the voltage step measurement. Extracting the feedback capacitance from the voltage amplification while taking the inject capacitance of 19.5 fF for granted, yields: C_f=19.5 fF/11.4=1.7 fF.

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[37] A misalignment of both layers, which form the capacitor, could explain the deviation.

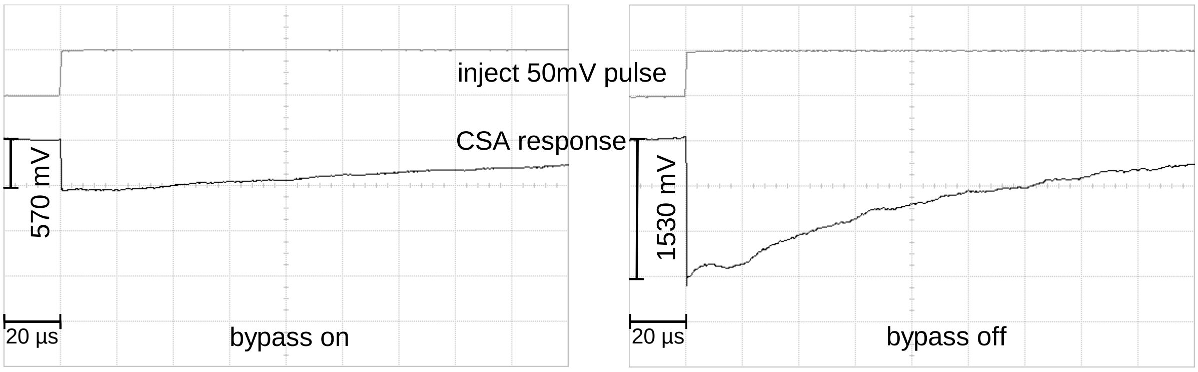

Figure 6.24 CSA response depending on feedback configuration

The effective feedback capacitance is extracted by comparing both cases as the bypass switch contributes additional capacitances, which are difficult to determine. From the voltage amplification without bypassing the effective feedback capacitance of C_{feff}=570 mV/1530 mV·2 fF=0.75 fF is extracted. Subtracting the DC-output of the CSA, the decay times can be extracted from a logarithmic plot of Figure 6.24. The decay times are 268 µs and 104 µs respectively. From the ratio of the decay times (assuming the same feedback resistance) an effective feedback capacitor of C_{feff}=104 µs/268 µs·2 fF=0.78 fF is calculated, which is in good agreement with the previously given value. To calculate the feedback resistance, one must consider that the capacitance seen by the resistor at the CSA input seems to be enlarged by the open loop gain A of the amplifier (see equation 8.26). Using the simulated open loop gain of about 16000, the feedback resistance hence is calculated: $R_{feed}=\tau/(A+1)\cdot C_f$=8.4 M$\Omega$. Using equation 8.23 and the emission coefficient n=0.5, a leakage current of $I=nkT/qR_{feed}$=1.5 nA is determined. A leakage current in the order of nA is confirmed by direct leakage current measurements on a probe station. The expected leakage current is 40 pA. A higher leakage current will result in larger noise. The deviation of the measured leakage current to the expected is justified by the fact that only some single pixels are bonded. The effective dimension of these pixels is enlarged over several pixels as shown in Figure 6.25; the larger area results in a higher leakage current.

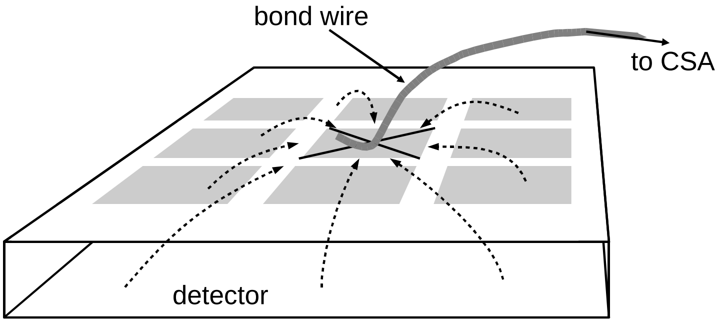

Figure 6.25 Charge generated below floating pixels flows to the CSA of a bonded pixel

Also optical tests have been performed. A bright light emitting diode (LED, 3000 mCd, 660 nm (red)) and a vertical cavity surface emitting laser (VCSEL, 850 nm (infrared)) are used to apply optical pulses to the detector as shown in Figure 6.26.

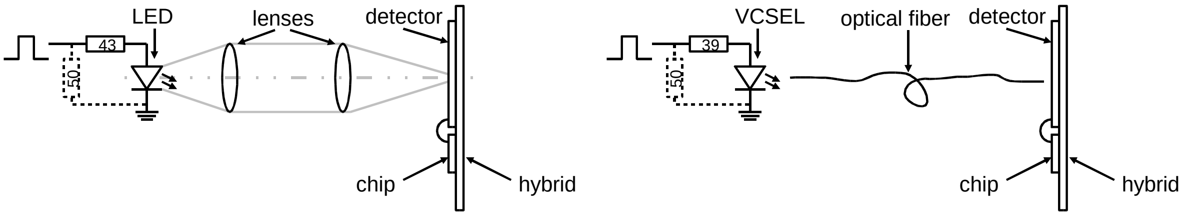

Figure 6.26 Setup to apply optical pulses

Different wavelengths are used to avoid errors due to the fact that the charge might be generated in a non-sensitive area of the detector. Figure 6.27 shows the absorption length in silicon at T=300 K [Gro 01].

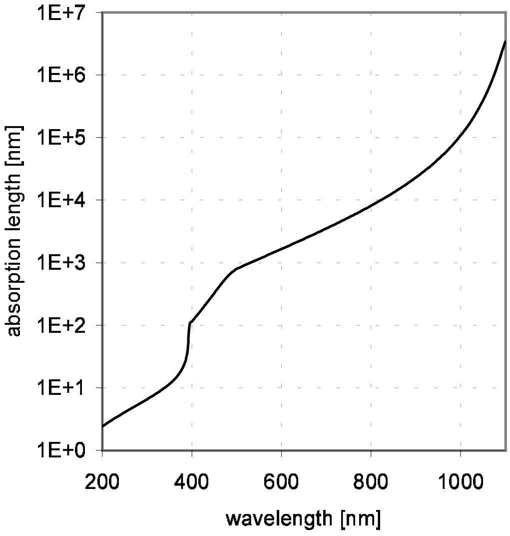

Figure 6.27 Absorption length in silicon (T=300 K)

The absorption length of the red light of the LED is 1.1 µm and for the infrared light of the VCSEL 13.2 µm respectively. A bigger part of the red light is therefore absorbed in the insensitive volume of the detector (thickness: several 100 nm).

The insensitive volume is decreased with increasing detector bias voltage. Figure 6.28 shows the amplifier response to a 100 ns-LED pulse. The light is coupled into the detector from the pixel side. The higher the depletion voltage, the more photons generate electron-hole pairs in the sensitive volume of the detector.

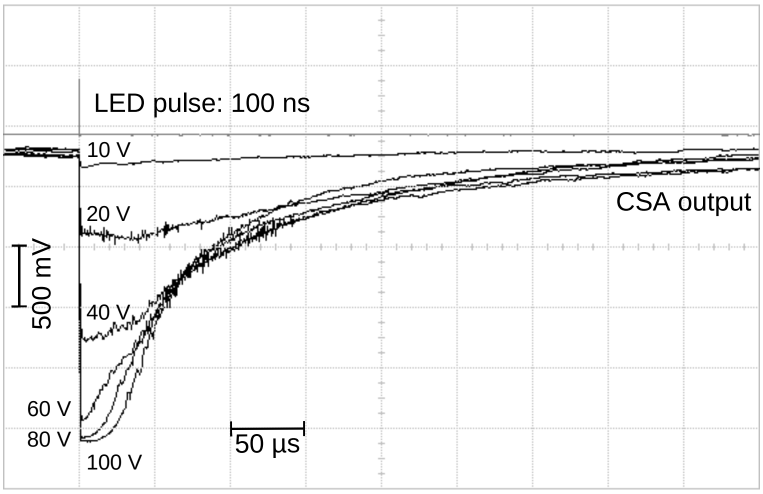

Figure 6.28 CSA response to a LED-pulse for different detector bias voltages

A similar result is obtained for a 10 ns-VCSEL pulse as shown in Figure 6.29.

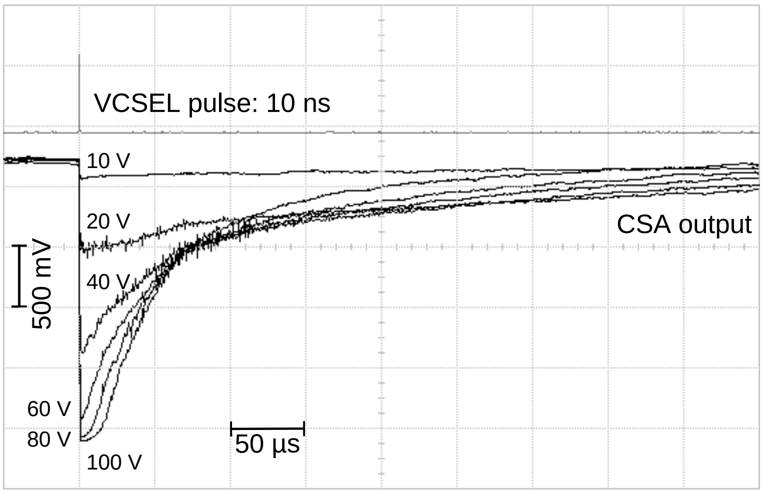

Figure 6.29 CSA response to a VCSEL-pulse for different detector bias voltages

A disadvantage of a higher detector bias voltage is the higher leakage current (shorter decay times), since the decay time should be several times larger than the shaping time. A quantitative analysis of the optical test pulses is difficult, since the fraction of photons injected to a pixel cannot be determined.

The response of the CSA to a double injection[38] is shown in Figure 6.30. Although the second pulse is superposed to the tail of the first pulse, the shaper distinguishes

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[38] A double injection cannot be performed by two pulses, because the trailing edge of each pulse injects charge of the opposite polarity. To achieve a double injection a step-function is applied by adding two delayed pulses.

both due to the shorter shaping time. The response for a single inject-signal is also shown in light grey.

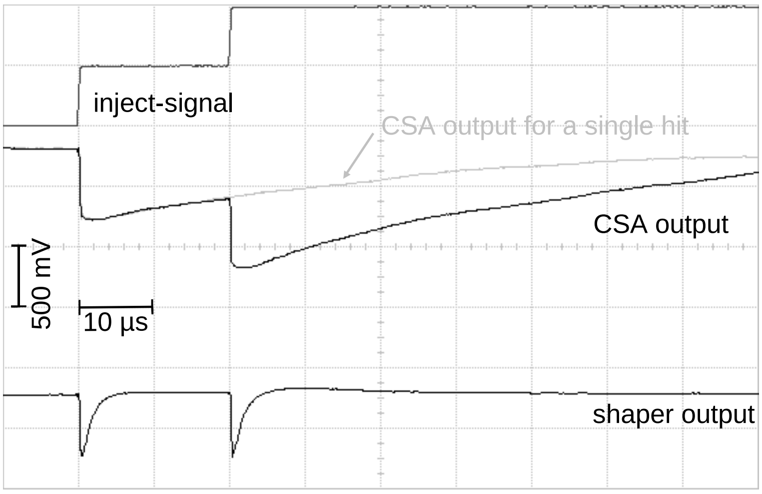

Figure 6.30 Two added pulses for double injection: CSA response and shaper output

To investigate the coupling of the detector bias noise, a test setup as shown in Figure 6.31 is used. Applying a voltage step of 16.6 mV to a capacitor (100 nF) causes an exponential rise of the voltage across the detector of 14.8 mV, which is measured with a probe (10 MΩ || 9 pF). The probe forms together with the 1 MΩ resistor a voltage divider of 10/11. This results in the lower voltage change (16.6 mV$\cdot$10/11=15.1 mV). The capacitance of the probe together with parasitic capacitances on the PCB and the detector capacitance causes the exponential rise ($\tau\approx$20 µs$\Rightarrow C\approx$20 pF).

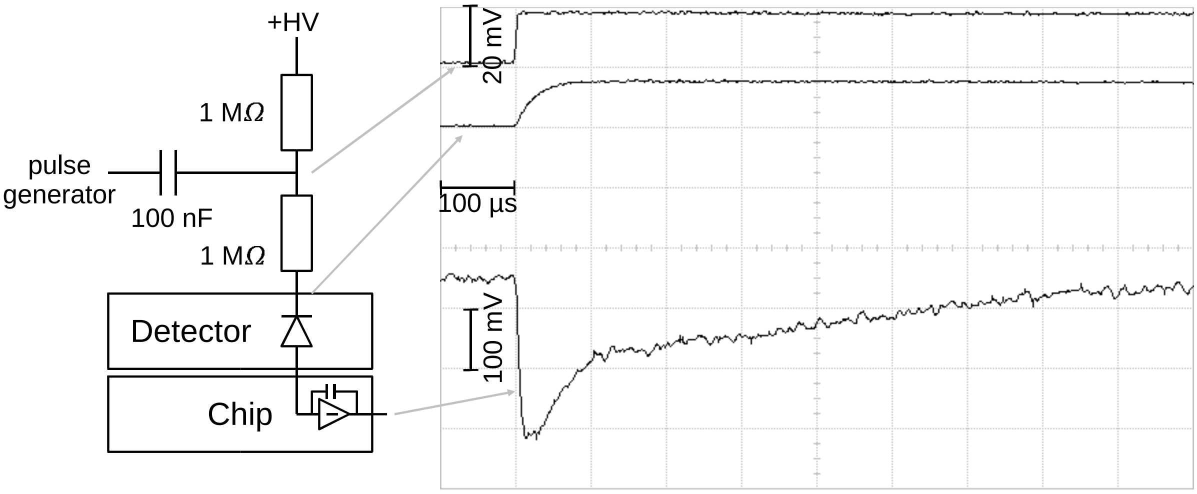

Figure 6.31 Charge injection via the detector bias (average of 16 measurements)

Applying electrical test pulses, after the exponential rise time has been reduced by bypassing the 1 MΩ-resistor next to the detector, both via the inject capacitor and via the detector gives an estimation of the pixel to backside capacitance. Figure 6.32

shows the CSA output for both injection methods. The pixel-to-backside capacitance is $C = C_{inj} \cdot 1250\ \mathrm{mV}/280\ \mathrm{mV} = 87\ \mathrm{fF}$.

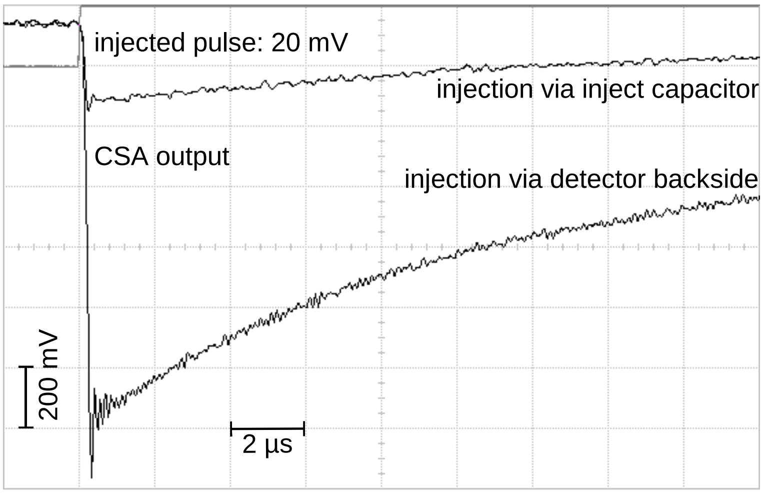

Figure 6.32 CSA response due to charge injection: Via inject-capacitor and via detector respectively

The pixel to backside capacitor is part of the detector capacitance. Additional capacitances are added due to the inter-pixel capacitors.

To achieve an operation of the wire-bonded pixels at all, the bulk voltage (V_{bulk}) is pulled to a higher voltage than V_{DDA}, which was foreseen to reduce the noise due to the influence of the parasitic JFET (see section 4.2.2). The measurements are done with $V_{bulk} \approx 6.5$ V. This fairly high voltage near the absolute maximum ratings of the process often causes latch-up (see section 8.2): The power supply has to be disconnected, V_{bulk} has to be connected to V_{DDA} and the system must be re-powered. Afterwards V_{bulk} again is connected to the higher voltage and the shift registers are rewritten again.

6.4.2 Shaper

To investigate the shaper dependence on the bias current (DAC 06/itau), a small electrical pulse (200 mV), which is divided by 10 on the PCB, is applied to the inject pad. The corresponding CSA output and the shaper output for different settings of the DAC are shown in Figure 6.33. To get rid of noisy spikes, an average of 16 measurements is plotted.

Not only the shaping time depends on the DAC-setting, but also the DC-offset: For larger currents the DC-offset decreases, which also decreases the maximal output swing (limited by ground level).

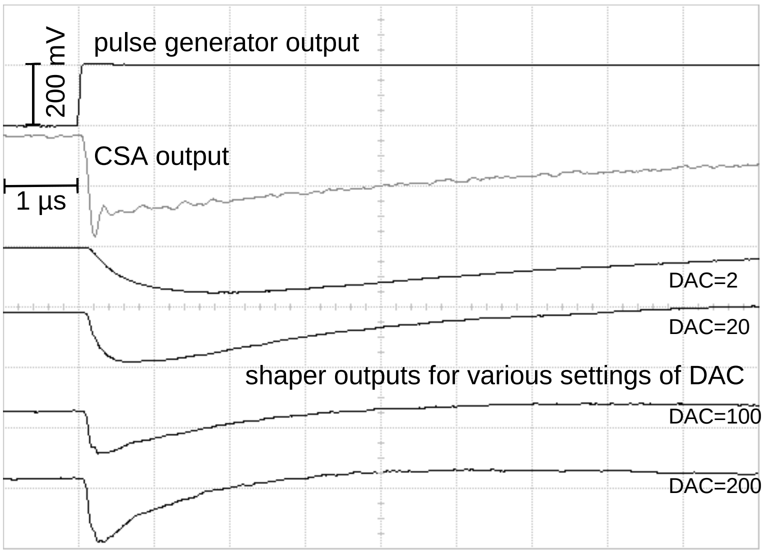

Figure 6.33 Shaping time dependence on DAC 06 (itau) settings; CSA and shaper outputs are averaged (16 measurements)

The DAC current is divided by 32 in the end-of-column and by 3 in each pixel. The calculated bias current in the shaper of each pixel is: DAC setting · 40 µA/(64 · 3 · 32). The shaping time for small signals is calculated by (see equation 4.43):

$$\tau = RC = \frac{C}{g_m} = \frac{1}{\sqrt{2I\frac{W}{L}KP_P}} \tag{6.8}$$

Table 6.7 lists the measured and calculated shaping times depending on the DAC 06 settings. The measured shaping times are in good agreement with the hand calculated values. For short shaping times the limited bandwidth of the output buffer modifies the signal.

DAC 06 (itau)	I [nA] (calculated)	τ [µs] (measured)	τ [µs] (calculated)
2	13	1.7±0.05	1.85
20	130	0.6±0.04	0.58
100	651	0.2±0.03	0.26
200	1302	0.2±0.03	0.19

Table 6.7 Measured and calculated shaping times vs. DAC 06

For larger signals (e. g. photo absorption), the shaping time cannot be adjusted by the DAC settings as shown in Figure 6.34.

A pulse of 1.8 V amplitude, divided by 10, injects charge into the CSA, causing an CSA output voltage of approximately 2 V. The output voltage of the shaper is also

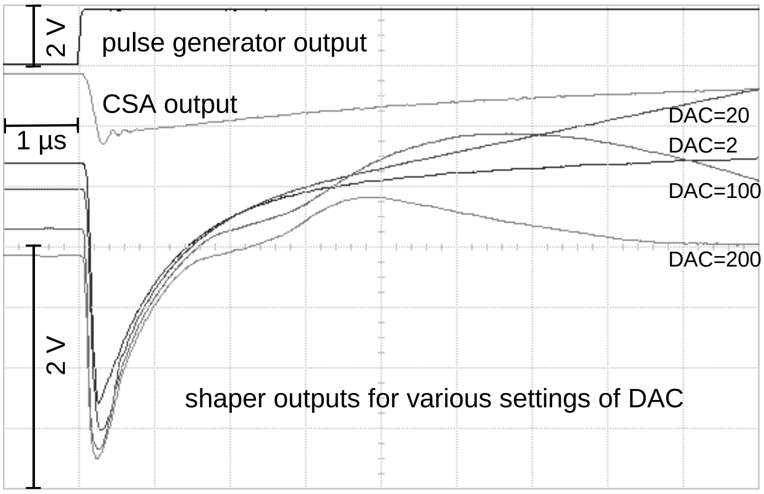

Figure 6.34 Large signal shaping time for different DAC 06 settings (averaged over 16 measurements)

about 2 V. In agreement with the simulation, the shaping time is independent of the DAC 06-setting.

The DC-levels of the shaper outputs of all pixels are shown in Figure 6.35 for two DAC settings: The higher the DC-current (high DAC 06-value) the lower the DC-level. The origin of the standard deviation (σ=55 mV) of both distributions is the threshold variation of both the current mirrors and the diode connected transistors, which form the resistive load of the shaper (see Figure 4.16). An additional offset comes from the offset voltage of the debug output buffers. No systematic error due to voltage drops across the supply line is seen.

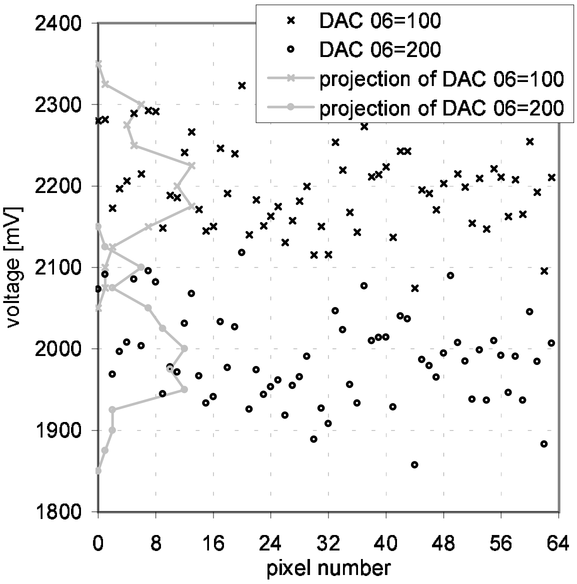

Figure 6.35 DC-level variation of the shaper for all pixels and two DAC settings

The pixel number corresponds to the pixel shift register: Pixel 0...31 corresponds to column 31...0 of the bottom row, pixel 32...63 to column 31...0 of the top row.

To estimate the noise of the system (Ramses 3), the shaper output level is measured, if no signal is applied. Figure 6.36 shows the shaper level for two different time scales[39] and a gaussian fit to both level distributions.

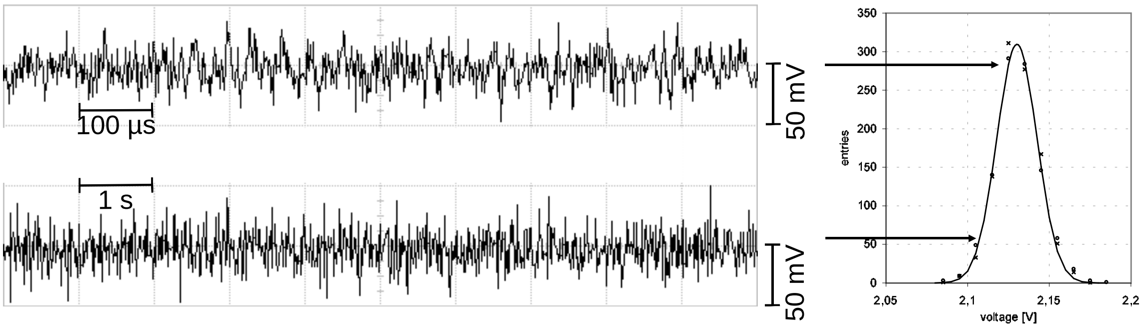

Figure 6.36 Shaper output due to noise for two different time scales; voltage histogram for both time scales and a gaussian fit to determine rms-noise

The standard deviation oft the gauss fit is σ=12.33 mV. With the calibration of this pixel (C_f=1.77 fF; 20 mV inject pulse⇒220 mV CSA signal⇒170 mV shaper signal), a rms-noise of 12.33 mV/170 mV · 2434 e=195 e is determined.

This fairly high noise is traced back to the higher leakage current. Additional noise comes from the higher parasitic capacitance (wire-bonds to detector) and the debug-output-buffers. By pulling the CSA-output to ground (DAC 05=0), the noise contribution of the output-buffer is determined: σ=2.58 mV⇒ENC$_{\text{buffer}}$=22 e. A proof that the noise is leakage current dominated is derived from Figure 6.37.

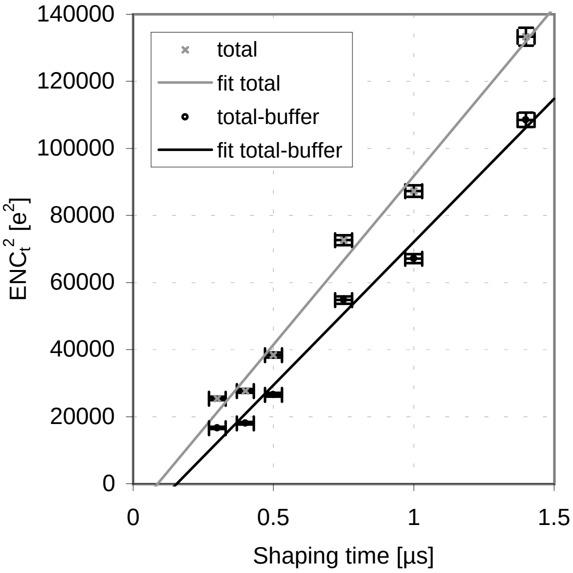

Figure 6.37 Measured total noise versus measured shaping time

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[39] Two time scales are used to watch out for low frequency noise (e. g. 50 Hz) as well.

The total noise rises with the shaping time, which indicates a leakage current noise (see equation 4.44). From the slope of a linear fit to $ENC_t^2(\tau)$ a leakage current of 3.4 nA is extracted (corrected by the buffer noise). This value has a large error due to the following reasons: The shaping time has a total error of 5 %, including both stochastic errors and systematic errors[40]. The error in the equivalent noise charge influences the extracted leakage current even more: The voltages to determine the noise are measured precisely to 1 % of their real value. A systematic error occurs due to an error of the calibration capacitor of 10 %, which translates to an error in ENC^2 of 20 %.

6.4.3 Peak Detector

Figure 6.38 shows the response of the peak detector to a shaper output pulse, if the discriminator has recognised a valid hit and the pixel is not masked. The upper plot shows the response for different peak detector bias settings (DAC 03). If the bias of the peak detector is to low (e. g. 50 DACcounts≈2 µA), it is to slow to recognise the extremum. The peak detector is sufficiently fast for a bias of 200 DACcounts≈8 µA. The optimal bias depends also on the shaping time. Larger shaping times require lower bias currents.

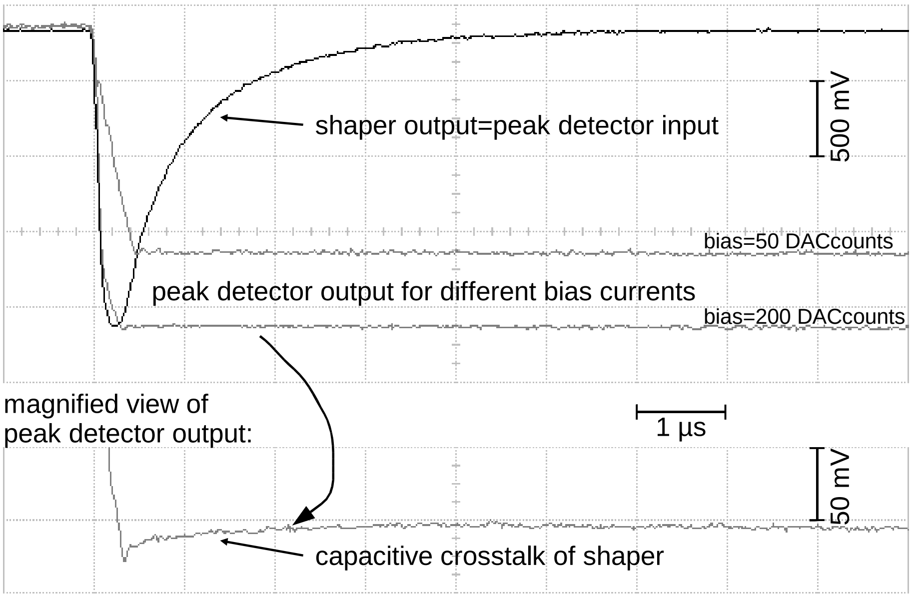

Figure 6.38 Response of the peak detector to a shaper signal

The lower plot of Figure 6.38 illustrates the capacitive cross coupling of the shaper output to the peak detector storage capacitor by the parasitic capacitance of the reset switch. The two volt shaper amplitude translates to a 20 mV peak detector voltage change. Assuming that the peak detector's storage capacitor meets the design value of 524 fF, a switch capacitor of C_{sw}=524 fF/(2 V/20 mV−1)=5.3 fF is calculated (according to equation 8.27), which is in the order of the parasitic capacitances of the reset transistor.

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[40] The time constants of the additional output buffers, the oscilloscope probe and the input of the oscilloscope contributes to a shaping time, which is larger than the pure CRRC-shaping time.

In Figure 6.39 the long time behaviour of the peak value is considered. The voltage across the storage capacitor changes with time due to leakage currents. For this reason the readout should start as soon as possible. Calculating the resulting leakage current, gives: $I_{leak}=C\cdot dU/dt=524\ \mathrm{fF}\cdot 200\ \mathrm{mV}/19\ \mathrm{s}=5.5\ \mathrm{fA}$. This leakage current depends on temperature, absolute voltage across the capacitor, voltage across the reset switch and illumination. The voltage change due to this leakage current during the intended readout time of 10 µs is with $\Delta U=I\cdot\Delta t/C=0.1\ \mu\mathrm{V}$ negligible. The capacitive cross coupling of the shaper output can be more likely a problem. Due to a certain amount a software correction can recalculate the correct value.

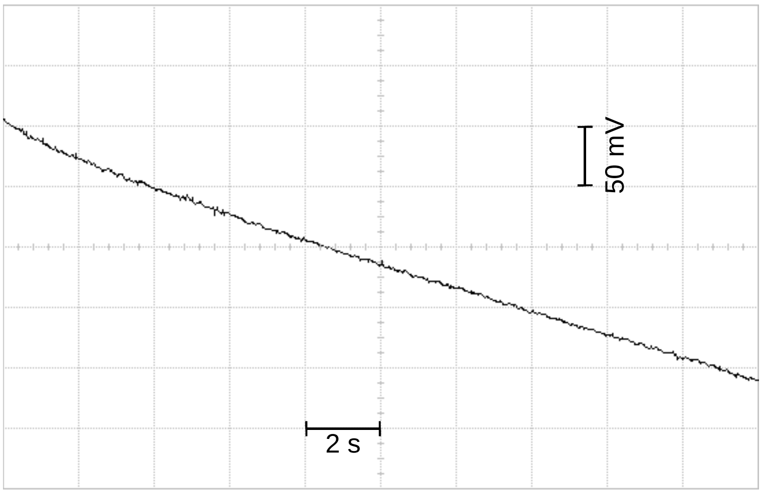

Figure 6.39 Change of the stored peak value due to leakage currents

6.4.4 Buffer

The response of the pixel buffer, which drives the bus with the peak detector voltage level while a pixel is selected, is shown in Figure 6.40. The peak detector output as the response to a hit is also shown. The discriminator discovers a valid signal and triggers the end-of-row and end-of-column logic. The XILINX™ starts automatically a delayed[41] (0.8...1.0 µs) readout cycle.

As soon as a pixel is selected on the falling edge of the clock signal, the analog buffer is enabled, driving the bus capacitance. Depending on the DAC settings (DAC 02 for pixel buffer bias, DAC 11/12 for output driver bias) a settling time below 300 ns is achieved.

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[41] A delay of four 5 MHz-clock cycles is implemented. Depending on the time between the hit-edge and the clock edge a jitter of maximal 200 ns can occur.

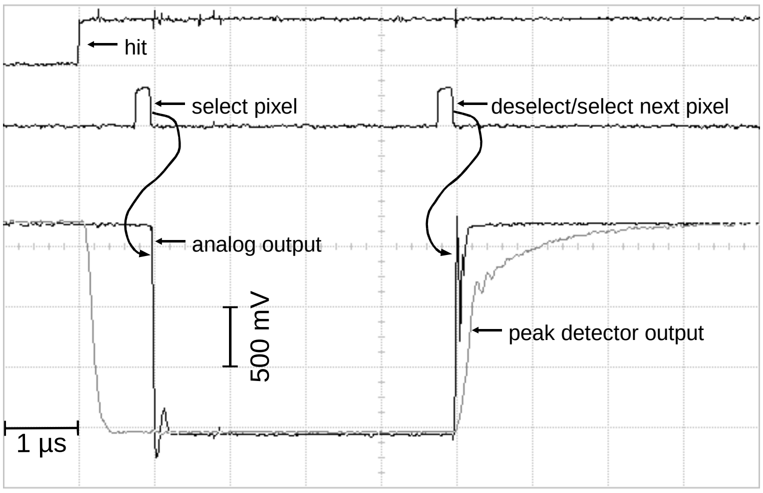

Figure 6.40 Readout triggered by a hit

6.4.5 Discriminator

To save pixel area, the discriminator is not AC-coupled to the CSA, but DC-coupled within the shaper (see Figure 4.20). Therefore the threshold of the discriminator depends not only on the supply voltage (resistances of transistors in triode region change with gate-source voltage) and shift register settings of the switches (5 bit), but also on the bias current of the shaper: A higher shaper bias current corresponds to a larger threshold step per bit.

The discriminator switching speed depends on the discriminator's bias current (DAC 08). For a large bias (DAC 08 set to 250), a delay between inject pulse and chip response (hit-bus or hit row) of 50 ns can be achieved, whereas for a DAC setting of 20 the delay increases up to 200 ns.

To characterise the discriminator, the threshold has to be determined. By injecting charge via the inject capacitor, the threshold can be determined: If the injected charge is below the threshold, then no hit is recorded, otherwise it is. Due to noise, the discriminator input voltage is blurred, which sometimes causes pulses, even if the injected charge is below the threshold, and on the other hand the discriminator sometimes records no hit, even if the injected charge is well above the threshold. To decide, weather a hit has occurred or not, the hit-bus line is used (see sections 4.10.1 and 6.5.2).

Since the noise amplitude is normal distributed, the probability of recording a hit corresponds to the probability density of a Gaussian distribution. The mean value is a measure for the threshold, the standard deviation for the noise amplitude.

To measure the probability density, several bursts of pulses are injected into the CSA. The relative frequency for each burst[42] with a fixed amplitude is measured and taken as probability[43]. If the burst amplitude is varied, the probability density versus injected charge is measured (referred to as threshold scan). Fitting the normal distribution density

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[42] A burst consists of a sequence of 127 pulses.

[43] For an infinite number of pulses in a burst, the relative frequency equals the probability. For a finite number, the probability is close to the relative frequency.

$$p(x,\mu,\sigma)=\frac{1}{\sqrt{2\pi}\,\sigma}\int_{-\infty}^{x} e^{-\frac{(t-\mu)^2}{2\sigma^2}}\,dt \tag{6.9}$$

to the relative frequency versus injected charge, one yields the threshold μ and the noise-amplitude σ.

The number of hits per burst is measured by means of the hit-bus. Since the smallest amplitude of the pulse generator into 500 Ω (see Figure 5.5) is 200 mV, the smallest charge, which can be injected, is relatively large[44] ($Q_{min}=C_{inj}\cdot U_{in}=19.5$ fF $\cdot$ 200 mV:10=0.39 fC=2440 e). Therefore to perform a threshold scan, the threshold must be set higher than 2440 e. A higher threshold is set by a higher bias current (DAC 06), which simultaneously reduces the shaping time, because the discriminator is embedded in the shaper circuit as described in section 4.4. A shorter shaping time results in a non-optimum noise performance.

Figure 6.41 shows threshold scans and the corresponding fits of the Gaussian probability density distribution for thresholds between 17 and 31 (PixelSR).

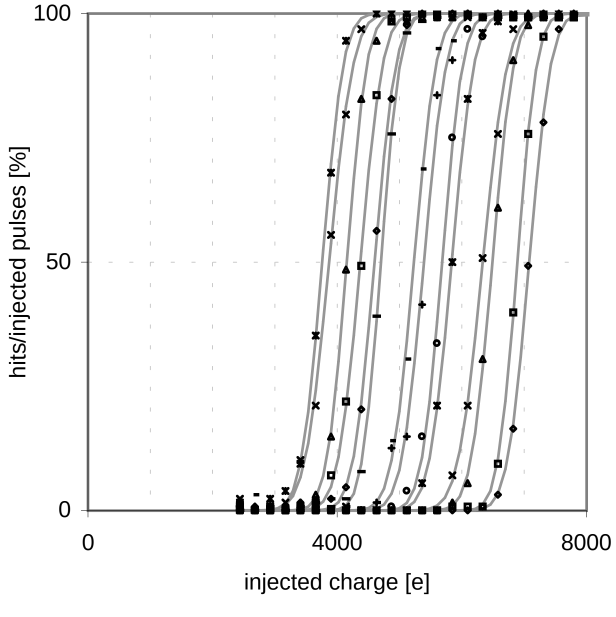

Figure 6.41 Threshold scans for different thresholds

Table 6.8 lists the parameters extracted from fits to the data of Figure 6.41.

The thresholds for the different settings are taken from the fits and they are plotted versus the digital code in Figure 6.42. A good linearity is visible, although some systematic deviation from linearity is also seen due to transistor mismatch[45]. With the high bias current (to achieve the high threshold), the threshold change per bit is also relatively large (260 e).

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[44] In a further revision an additional inject capacitor, which is about 10 times smaller, should be taken into account to perform threshold scans with even lower thresholds.

[45] To provide a larger threshold, longer transistors are used. The resistance of a transistor in triode region is only in first approximation proportional to the length of the transistor. Due to second order effects, doubling the transistor length neither doubles the resistance nor the threshold.

dig. thresh. code	threshold µ [e]	noise σ [e]
17	3545	278
18	3762	268
19	3872	306
20	4156	255
21	4373	283
22	4601	272
23	4704	239
24	5234	281
25	5393	283
26	5687	261
27	5840	283
28	6339	313
29	6492	272
30	6894	246
31	7084	275
mean threshold change per bit	260	
mean noise		274

Table 6.8 Parameters from fits to data in Figure 6.41

The higher noise subsumed in Table 6.8 compared to the noise extracted in section 6.4.2 is traced back to a non-optimum shaping time (both high DAC 06 current and large signals reduce the shaping time) and additional noise introduced by the external resistive voltage divider.

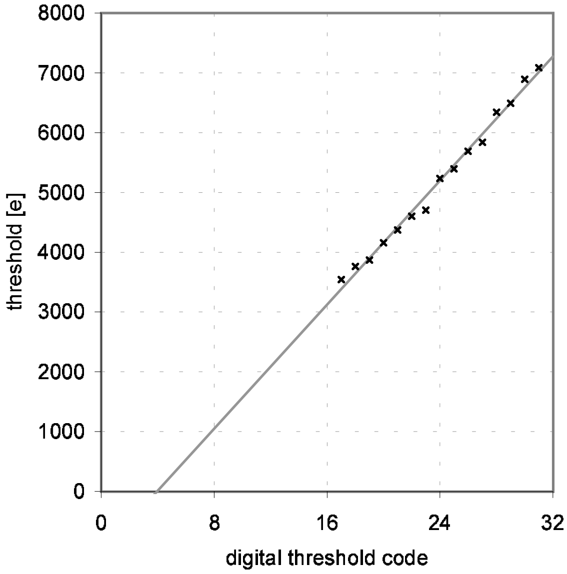

Figure 6.42 Threshold dependence on settings

To check for a threshold dispersion across the chip, the thresholds of five[46] bonded pixels for the same threshold settings are shown in Figure 6.43.

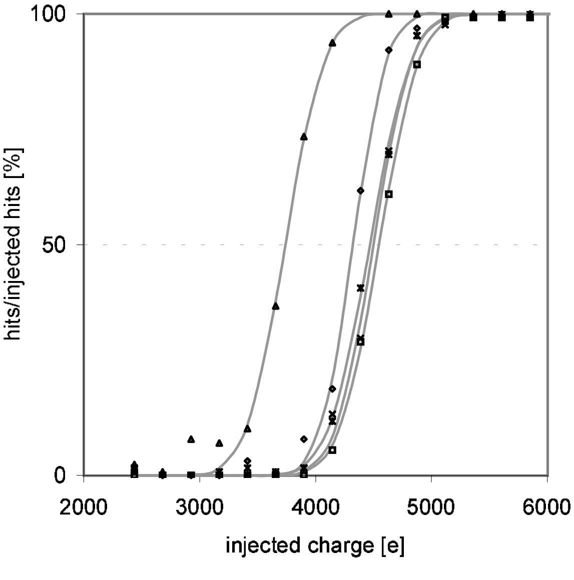

Figure 6.43 Threshold scans for different pixels

Except one threshold, the four other thresholds are within 100 electrons spread. The threshold dispersion includes the variation of the inject capacitor, the variation of the feedback capacitor (and capacitive divider) and an offset error in the differential stage of the discriminator.

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[46] On a second hybrid, a further chip and detector were (wire-) bonded. Five pixels of the detector could have been connected.

6.4.6 Time-to-Voltage Converter (TVC)

Two currents are responsible for the proper operation of the TVC (see section 4.8):

- sfbias (DAC 00): Active load of the source-follower output of the TVC. The pixel current is 1/16th of the DAC output current.
- tbias (DAC 01): Time base current. The larger the current, the smaller the time range and the higher the resolution. The DAC current is divided by 64 in the end-of-column and by 2 in each pixel. A division in the pixel reduces mismatch, since the local matching is better than the global.

The voltage across the capacitor in the TVC is shown in Figure 6.44 for various time base currents (DAC 01). Extracting the capacitor from the slew rate (DAC 01 set to 240: I=39.6 µA·240/(64·64·2)=1.16 µA) yields $C_{TVC}=I/(dU/dt)$=1.16 µA/(1.076 V/µs)=1080 fF, which is in perfect agreement with the designed capacitor value of 1085 fF. This shows not only the excellent capacitor modelling and processing, but also a good current mirror matching for moderate currents. For small currents this matching gets worse: up to 20 % mismatch for I=24 nA (DAC 01 set to 5).

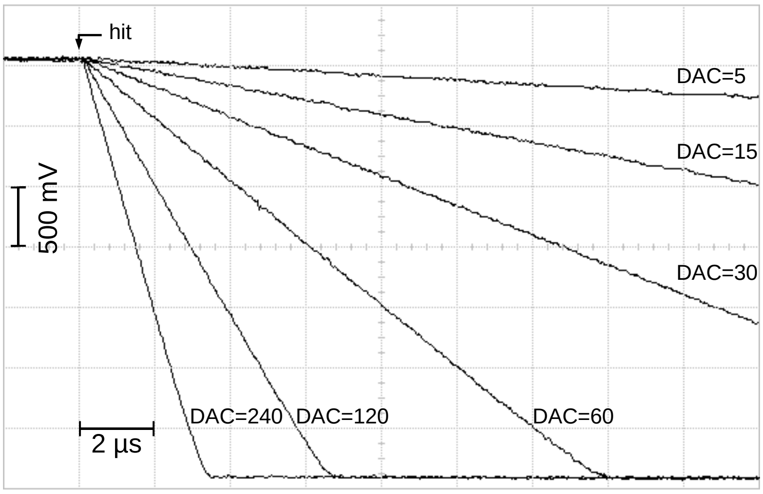

Figure 6.44 Voltage across TVC-capacitor for different bias currents

From the linearity of each slope of the capacitor voltage the high quality (large output resistance) of the current source is concluded. Since the output driver of the TVC is a simple source follower as the area in a pixel is limited, a voltage drop to the output has to be accepted. Figure 6.45 shows both the voltage across the TVC-capacitor for different delays between hit and readout (left diagram) and the output voltage of the source-follower (right diagram) for a time base current of 290 nA (DAC 01 set to 60). The pixel is selected after a certain delay to the hit. A selection of a pixel stops the time measurement, since the time difference between hit and readout time is going to be measured. At the same time the TVC-source-follower drives the internal bus to transfer the voltage, which is correlated to the elapsed time, to the external ADC. From the right plot a settling time of 300 ns is determined.

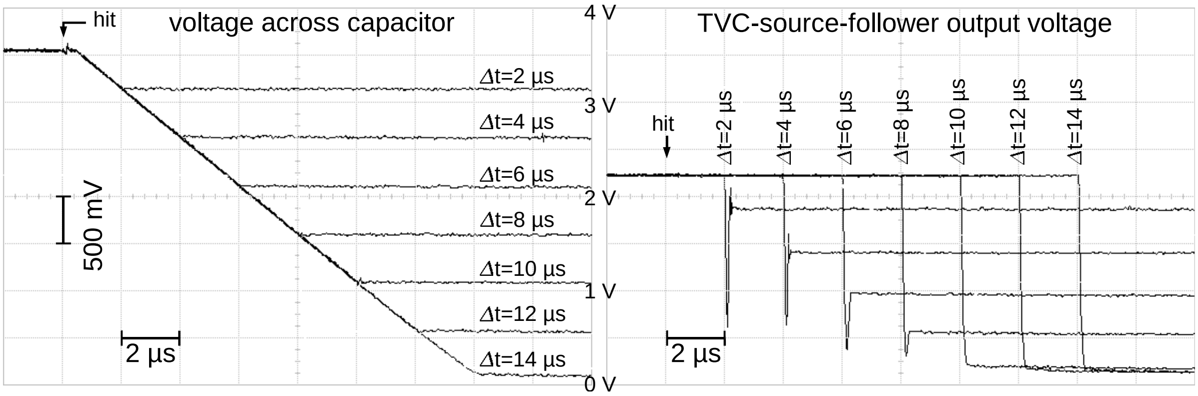

Figure 6.45 Voltage shift due to source-follower

Although the voltage across the TVC-capacitor can reach any voltage between ground and V_{DDA} (here 3.60 V), the sensible range is limited to those voltages, at which the source follower properly works. From the right diagram an operating range up to Δt=10 µs (for DAC 01=60) is determined. The body-effect of the NMOS-source follower requires a calibration of each TVC for precise time measurements. From the reproducibility (< 15 mV) of the output voltage for a given delay range of 10 µs, a resolution of better than 50 ns in 10 µs is estimated.

The leakage current, which discharges the TVC-capacitor after a stop signal has been measured: For a dark environment (setup covered with a black blanket) the voltage across the capacitor changes by 36.8 mV in 9.2 s. The leakage current is $I_{leak}=C_{TVC}\cdot dU/dt$=4.3 fA. If the blanket is removed and the electronic chip therefore is exposed to light, a five times larger leakage current is observed.

6.5 Performance of Column/Row Logic

Referring to sections 4.12 and 4.7 the performance of the EOR logic and EOC logic is shown in this section. Also measurements of the hit-bus system as described in section 4.10.1 will be presented.

6.5.1 Hit-Column/Hit-Row

The bias current for the end-of-column/-row hit-bus system is set by DAC 13 (hit-row/column bias). No current (DAC 13 set to 0) disables the end-of-column and end-of-row-logic. All other values are measured to result in the same response time, which makes this DAC setting uncritically. The delay time between hit and hit-column/hit-row signal is approximately 50 ns. The DAC setting only has an impact on the delay between the selection of a pixel and the reset of the hit-column/hit-row bus: The larger the bias current, the faster the reset: A DAC setting of 240 results in a delay of 50 ns for hit-row-reset and 30 ns for hit-column-reset[47], a setting of 10 results in a delay of 500 ns for hit-row-reset. The delay of the hit-column-reset remains at 30 ns. A complete measured timing diagram for automatic readout is shown in Figure 6.46:

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[47] Only two pixels form a column, but 32 form a row, which results in a different delay due to different load capacitances.

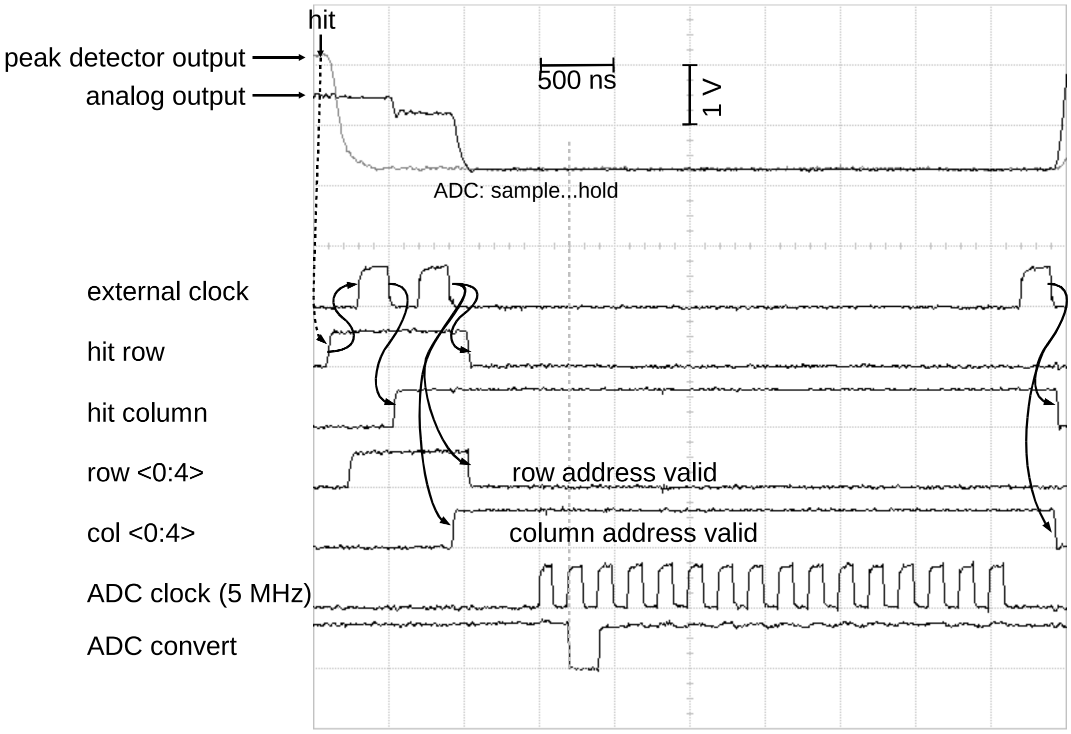

Figure 6.46 Timing of the end-of-row/column logic

As soon as a hit has been detected by the un-masked discriminator, the hit-row signal goes high, initiating the XILINX™ to start the readout cycle. The falling edge of an external clock pulse, provided by the XILINX™, selects the corresponding row. The pixel with the hit notifies the end-of-column logic, which drives the hit-column line. Another clock pulse selects the pixel for readout: The peak detector voltage and the TVC-voltage are routed off the chip to be sampled by the external ADCs. The peak detector voltage at the output pad is shown as 'analog output'. As soon as the pixel has been selected, its address (column and row) is provided at corresponding output pads. After a programmed delay time, which allows the analog output buffer to settle, the ADC readout sequence is started: A burst of 16 pulses of a 5 MHz clock and the conversion signal (ADC conversion low during the second falling edge of the clock pulses) is generated by the XILINX™. The serial data stream of both ADCs (3 bytes), the address of the pixel (column and row: 2 bytes) and a time stamp[48] (3 bytes), which is generated inside the XILINX™, are stored in a FIFO: A whole event occupies 8 bytes.

The sparse scan of the pixel matrix works automatically (as shown in Figure 6.46), whereas the explicit manual selection of an arbitrary pixel only works, if at least one pixel has detected a hit, because the select line is tied to the hit line as shown in Figure 4.43. If no hit at all has occurred, the EOR logic does not start selecting a row. This deficit was overseen in the design phase, but can simply be fixed by an additional OR-gate[49] as shown in Figure 6.47.

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[48] The time stamp is generated from a 5 MHz clock and a 24 bit binary counter.

[49] Of course the same arrangement has to be implemented in the EOC logic as well.

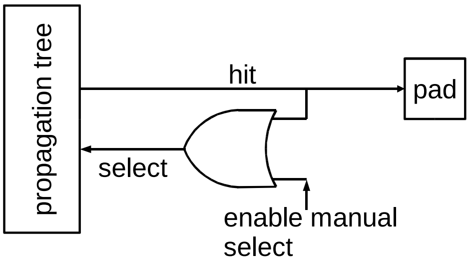

Figure 6.47 Minor correction to ensure always manual selection

The manual selection of a pixel exists only for testing purposes. Since the automatic selection works, a readout cycle is initiated without manual selection. Within less than 50 ns a row or column of a pixel, which has registered a hit and has notified the end-of-column/row logic, can be selected by an external clock pulse. Two pulses are required to select a single pixel: One pulse to select the corresponding row, another pulse to select the corresponding column. If more than one pixel per row was hit, only one additional readout pulse per valid hit is required.

6.5.2 Hit-Bus

The hit-bus is a wired-OR of all discriminators of non-masked pixels. An active load is formed by a current source, which is controlled by DAC 14 (hit-bus bias). Setting this DAC 14 to 0, disables the hit-bus system. For values between 1 and 170 the hit-bus system responds within 50 ns (DAC 14 set to 1) and 220 ns (DAC 14 set to 170).

A problem of the hit-bus system is a feedback to the CSA. If the hit-bus is enabled, spikes occur in the CSA-output as shown in Figure 6.48. A coupling within the pixel, e. g. from discriminator, is excluded, since the discriminator switches, even when the hit-bus is disabled. These spikes are reduced by a lower power supply voltage of the digital output buffer (V_{DDDBUF} can be reduced to 1 V). A capacitive coupling on the PCB to neighbouring lines has been observed as shown in Figure 6.49: If the hit-bus level changes, then a signal is couple to the enable-input line. From the decay time (140 ns) and the protection resistor of 4.7 kΩ between XILINX™ and PCB (see section 5.1) a capacitance between both lines of 30 pF is extracted.

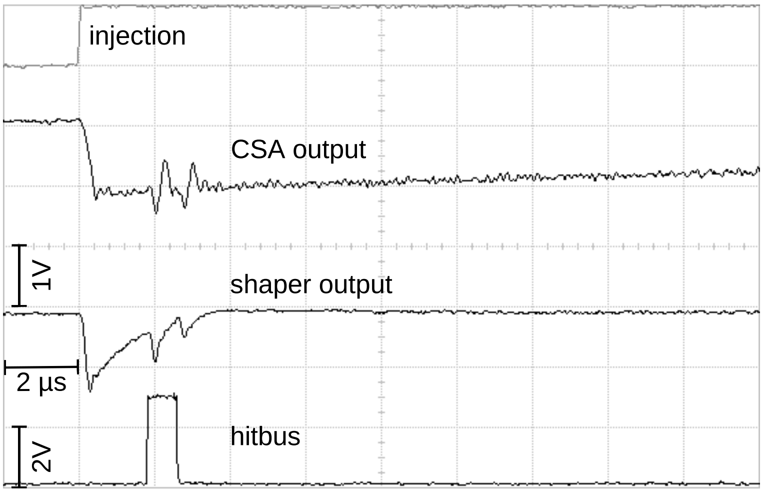

Figure 6.48 Switching of the hit-bus pad feeds back to the CSA

By limiting the voltage swing by means of a diode, the coupling and the crosstalk of the hit-bus is reduced to a great extent. In a further chip revision a low-voltage output swing or an open drain output for the hit-bus should be used.

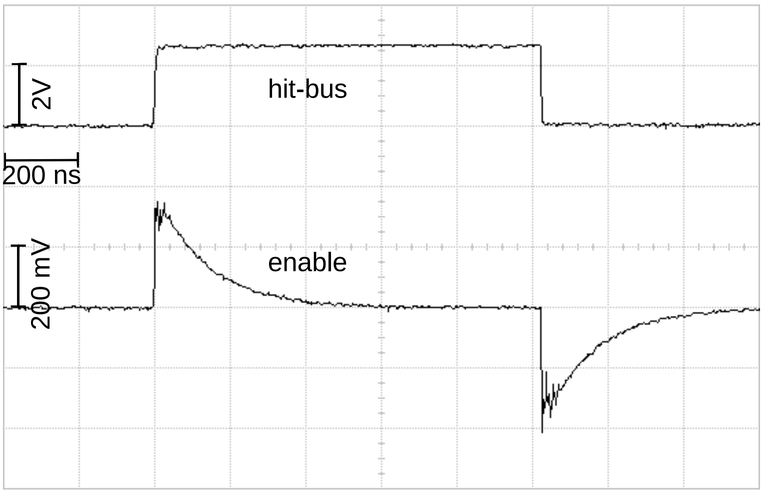

Figure 6.49 Capacitive coupling of hit-bus-output to enable-input on PCB and hybrid

This feedback of digital signals turned out to be problematic for the discriminator measurements. Therefore for threshold scans a digital filter was implemented within the XILINX™. To avoid crosstalk between adjacent traces, a proper shielding by intermitting ground traces, which reduce the capacitive coupling between signal traces, must be assured in a revised PCB design. Also optocouplers beside differential signal transmission to separate the ground levels and the digital noise of the XILINX™ should be taken into account.

6.6 Measurements with X-rays in a Single Pixel

To verify the electrical and optical tests, the detector was exposed to an X-ray source. A four year old ^{109}Cd-source (0.1 mCi @ 1997, $T_{1/2}$=462.6 d → 4.3 µCi=160 kBq @ 2001) has been used. The mean occupancy per pixel (50 µm × 450 µm=22500 µm) by the 5 mm distant source is therefore about 10 Hz.

	energy [keV]	intensity [%]	Assignment or decay mode	weighted mean energy [keV]
X-rays	2.984	4.57	Ag $L_{\alpha1}$	3.045±0.057
	3.151	2.64	Ag $L_{\beta1}$	
	21.990	29.511	Ag $K_{\alpha2}$	22.103±0.058
	22.163	55.720	Ag $K_{\alpha1}$	
	24.912	4.76	Ag $K_{\beta3}$	25.006±0.105
	24.943	9.23	Ag $K_{\beta1}$	
	25.455	2.308	Ag $K_{\beta2}$	
γ	88.045	3.61	ε	88.045

Table 6.9 Most important X-rays from ^{109}Cd [Chu 99]

Table 6.9 gives an overview over the most important X-rays emitted by ^{109}Cd [Chu 99]: The ^{109}Cd decays by an electron capture to an excited ^{109}Ag, which subsequently emits X-rays of the binding energy of the refilled shell of the captured electron (most probably K-shell). Since the resolution of the presented detector system is to small to resolve all energies, the weighted[50] mean value of some lines are given in the last row of the table.

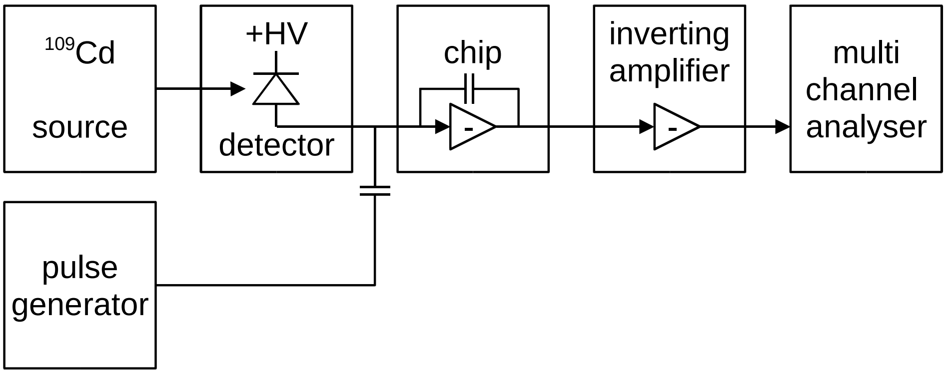

Figure 6.50 Setup for measuring the spectrum of ^{109}Cd

In Figure 4.49 the setup for the measurement of the spectrum is shown. Either signals generated by detected X-rays or electrical test pulses are used. The CSA and

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[50] weighted by the intensity

CRRC-shaper of the chip are used to amplify the signal. Since the output of the shaper is a negative pulse, an additional external inverting amplifier is used to form a positive pulse, required by the subsequent multi-channel-analyser (MCA).

The recorded spectrum of ^{109}Cd is shown in black in Figure 6.51. Also the response to the electrical test signals are plotted in grey. A magnified view of the peaks are also shown. To determine the mean channel of the peaks, gaussian distributions are fitted with a local linear underground.

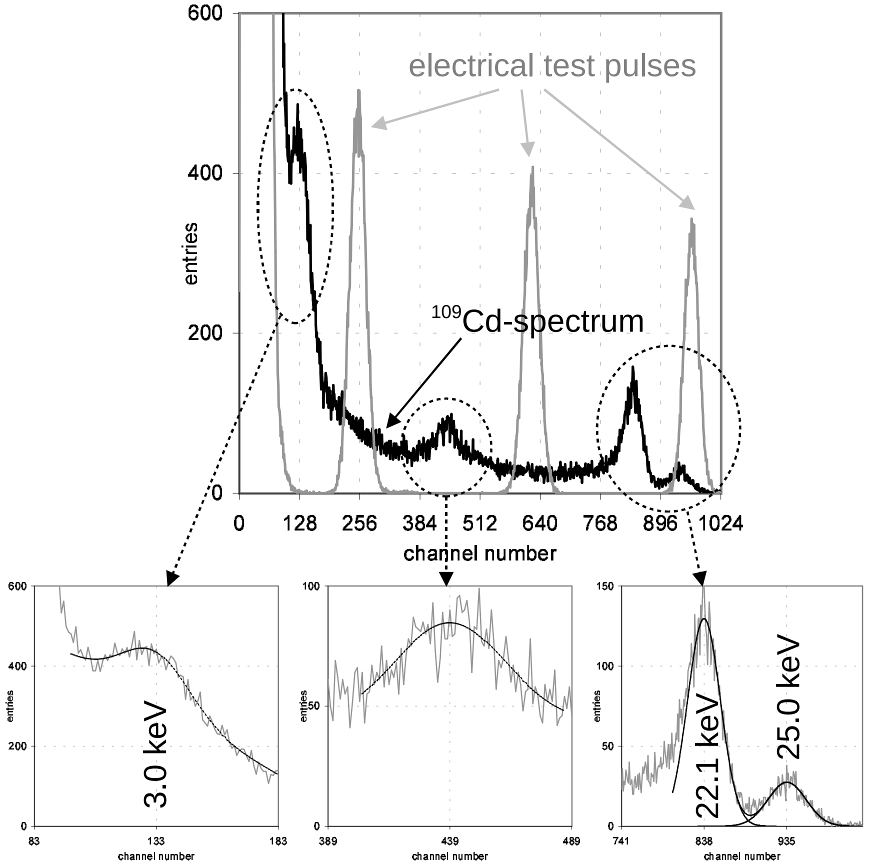

Figure 6.51 Spectrum of ^{109}Cd including injected electrical test pulses; magnified view of the peaks

The important parameters of these gaussian fits are shown in Table 6.10. Three energies could have been assigned to the Cd-source. A linear regression of the channel-energy relation gives: E(channel)$=-0.64063$ keV$+0.027292$ keV$\cdot$channel

With the slope of 0.027292 keV the rms-noise is calculated by multiplying by the standard deviation of the gaussian distributions. In silicon a mean energy of 3.63 eV is needed to generate an electron-hole pair (see Table 3.1). Therefore the equivalent noise is calculated by dividing the noise [eV] by 3.63 eV. Table 6.10 lists the calculated noise values as well. The corresponding energies of the injected pulses are calculated from the above equation.

Extracting the energy of the middle peak (channel number 439), the linear energy-channel relation is used. An energy of 11.34±0.06 keV is calculated. It is probably a X-ray fluorescent peak of the gold plated copper traces of the hybrid board, which carries the detector.

	channel number	σ	corresponding energy E [keV]	noise [eV]	noise [e]
^{109}Cd souce	132.8±1.0	13.9±1.3	3.045	379	104
	439.0±1.0	22.9±1.3		624	172
	837.8±0.3	19.4±0.8	22.103	529	146
	935.4±0.7	22.3±1.0	25.006	608	167
electrical injected charge	252.52±0.14	16.88±0.14	6.290	461	127
	621.42±0.18	16.90±0.18	16.33	461	127
	961.65±0.21	15.63±0.21	25.60	427	118

Table 6.10 Extracted channels of the peaks and determination of equivalent noise

The fit to the first peak is a bit complicated, because of the background. Therefore its standard deviation seems to be a bit to small. The mean noise according to the other three peaks is 162 electrons. The mean noise of the electrical test signals is 124 e. The difference is caused by fluctuations of the number of electron-hole pairs generated in the detector and by the fact that X-rays of at least two different energies are the origin of each peak. The theoretical energy-dependent resolution due to fluctuations is given by [Gru 93]:

$$\frac{\sigma(E)}{E} = \sqrt{\frac{F \cdot W}{E}} \tag{6.10}$$

The Fano factor F and the mean energy necessary for generating an electron-hole pair W are listed in Table 3.1. The theoretical detector resolution $(\sigma(E)/E)$ of a silicon semiconductor detector for 25 keV is therefore $4 \cdot 10^{-3}$. The measured detector resolution is four times larger:

$$\Delta_{detector} = \sqrt{\Delta_{total}^2 - \Delta_{electrical}^2} = \frac{\sqrt{(608\,\mathrm{eV})^2 - (450\,\mathrm{eV})^2}}{25\,\mathrm{keV}} = 16 \cdot 10^{-3}$$

The higher detector resolution might be explained by the pixel geometry: Some charge flows to a neighbouring pixel and does not contribute to the signal – an effectively lower energy is reconstructed.

7 Summary and Outlook

A short summary of the developed readout system and an outlook will be given in this chapter.

7.1 Summary

The development, design and evaluation of an analog low noise readout for semiconductor pixel detectors has been presented. The radiation detection technique based on pixel semiconductor (particularly silicon) detectors examined here is a true spin-off from developments in high energy particle physics. Both the self-triggered readout and the access to precise analog energy information differ from the demands in particle physics and need appropriate modifications in the integrated electronics.

Some simulation results and the limits of the simulation were presented. The layouts of several blocks have been presented. Finally the measurements and performance of the fabricated chip showed promising results. The control of the chip by an appropriately programmed XILINX™ and a proprietary software have been shortly introduced. The electrical measurements were finally proven by a taking a spectrum of a ^{109}Cd-source. Table 7.1 summarises the noise figures taken from different measurements and even from different setups (see footnote on page 115).

measured noise [e]	method	section	comment
13.7	measurement of shaper output fluctuations for several injected pulses	6.4.1	Ramses 1 without detector (no detector leakage current)
195	shaper output signal without any applied signal	6.4.2	Ramses 3 with detector (only a few pixels are bonded)
274	threshold scan	6.4.5	non-optimum shaping time (large signals, high DAC 06 current)
124	electrical charge injected	6.6	including detector leakage noise
162	^{109}Cd source	6.6	including detector leakage noise and Fano-noise

Table 7.1 Summary of noise measurements

The dominant noise source seems to be an excessive leakage current (in the order of nA instead of several ten pA) of the prototype detector. This temporary solution has been chosen to overcome the technology problems of bump bonding a detector to a single chip (see page 21). The wire-bond connection also adds additional capacitance, which results in a large noise. The effective pixel size is also not well defined, since the adjacent pixels to the pixel under test are floating (not bonded).

From the noise point of view it is difficult to judge, weather the presented electronic is adequate to built a Compton camera. Measurements with dedicated pixel detectors – bump-bonded to the detector – therefore have to be performed.

To determine the optimum energy range of the incident photon, other limiting factors as the Doppler-effect (see page 10) and the energy resolution due to fluctuations (Fano-noise, see equation 6.10) have to be taken into account. From the medical point of view nothing contradicts the application of high energetic photons.

In all systems a compromise between low power, low noise and high speed must be made. On one hand the small size of the pixel structure limits the maximum power, while on the other hand reduces also the mean rate per pixel, which leads to moderate speed requirements. A low noise readout for imaging systems ideal for imaging with radioactive isotopes has been presented. The system is relatively simple to handle, since no cooling is needed and no complicate gas-system is used.

7.2 Outlook

The outlook will give the next steps in the development of a first prototype of a Compton camera based on silicon pixel detectors.

First of all an appropriate pixel detector must be bump-bonded to the chip to verify the low noise capability of the electronics with low leakage currents. For a proof of principle a silicon detector should be used as Compton scattering detector. The detection of the scattered photon (photo absorption) will be realised with a caesium-iodide (CsI)-crystals, which are read out by a pin diode array. In a further step this second detector can be replaced by the electronic chip bonded to a high Z-detector (GaAs, CdTe). This is one of the advantages of a hybrid-system: Both, the detector and the electronic chip, can be developed in a common and appropriate technology to achieve the optimal performance for each of them.

A revision of the preamplifier as shown in Figure 7.1 has to be implemented to overcome the relatively large drain-source leakage current of T_f, which is not properly simulated. By reducing the drain-source voltage, the current is also reduced. This is achieved by using the output of the CSA as drain voltage of T_f, since the CSA output level is approximately the input voltage level. Alternatively the drain of T_f can be connected to the reference voltage, which is externally applied and slightly below the operating point of the CSA.

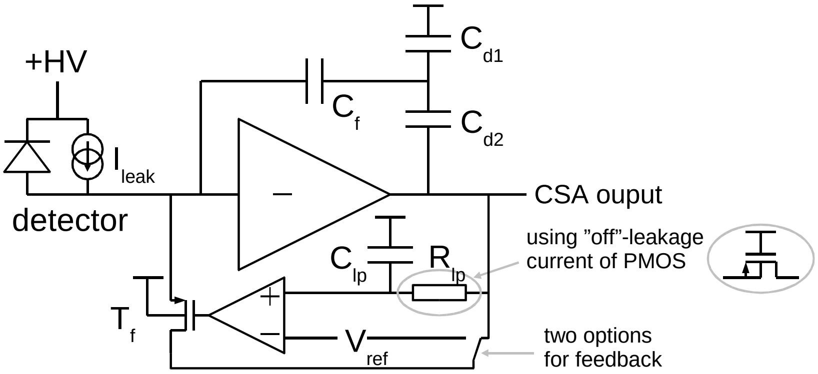

Figure 7.1 Improved CSA feedback topology to overcome simulation deficits

A new revision of the chip will be used to fix minor bugs, e. g. the possibility for manual selection of an individual pixel as mentioned in section 6.5 and the correction of the reference bias current (section 6.2.1).

Implementing small diodes, which can be switched to the CSA input, within the pixel, offers the possibility of testing with light pulses without the need for a bonded detector. The single chip bonding of the detector to the electronic chip is still a technological challenge.

In a next step one will aim for a larger sensitive area (e. g. 2×2 cm^2) by a composition of single chips and detectors. A batch of several layers can offer a higher detection efficiency, if necessary.

The reconstruction algorithms, which are continuously improved by several working groups, have to be adapted to the present environment. Measurements with phantoms will be done.

For precise measurement of the energy resolution at high rates and Doppler broadening at low energies (10 keV...30 keV) also synchrotron radiation, e. g. at DESY in Hamburg, will be performed.

Before a Compton camera based on silicon pixel detectors will come into medical operation, a lot of work has to be invested.

Although the research and development of the integrated readout electronics was done with respect to build a Compton camera, other applications, e. g. in two dimensional resolved spectroscopy, form possible fields of interest, in which an analog readout can be used.

Another possible alternative for very low noise[51] analog pixel readout offers the implementation of the first stage of the charge sensitive amplifier within the detector. This concept of the DEPJFET (depletion junction field effect transistor, [Lut 99]) to built a Compton camera will be followed.

---

[51] Low noise can be mainly achieve by reducing the leakage current and input capacitance of the detector: A very small internal gate, which is implanted within the detector, controls the current through a JFET. The change in current corresponds to the deposited charge. Different feedback mechanisms are still under investigation.

8 Appendix

This chapter should act as a quick reference. A short introduction to CMOS is given in the first section together with the fundamental equations for hand calculations. Basic circuits, both analog and digital, based on MOSFETs are presented in the second section. The third section gives an overview of the important noise sources appearing in semiconductor detector readout electronics. The fourth section serves as an overview of the specifications of the three chip versions. In the last section some physical constants, needed in the CMOS business, are tabulated.

8.1 Basic Structure of a MOSFET and Principle of Operation

The n-type metal-oxide-semiconductor field-effect transistor[52] (MOSFET) consists of a source and a drain, two highly conducting n^+-type semiconductor regions, which are isolated from the p-type substrate by reversed-biased pn-diodes. A metal (or poly-crystalline) gate covers the region between source and drain, but is separated from the semiconductor by the gate oxide. The basic structure of an n-type MOSFET and the corresponding circuit symbol are shown in Figure 8.1.

As can be seen in the figure the source and drain regions are identical[53]. It is the applied voltage, which determines the n^+-type region providing the electrons and becoming the source, while the other n^+-type region collects the electrons and becomes the drain. The voltages applied to the drain and gate electrode as well as to the substrate by means of a back contact are related to the source potential, as also indicated in the figure.

---

[52] The n-type or n-channel MOSFET will be primarily discuss. This type of MOSFET is fabricated on a p-type semiconductor substrate. The complementary MOSFET is the p-type or p-channel MOSFET. It contains p-type source and drain regions in an n-type substrate. The inversion layer is formed when holes are attracted to the interface by a negative gate voltage. While the holes still flow from source to drain, they result in a negative drain current. CMOS circuits require both n-type and p-type devices

[53] Individual MOSFETs, which are commercially available in a metal can or molded plastic package, frequently contain a connection between the source and the back contact so that the source and drain contact cannot be readily interchanged. For this reason, the bulk contact is often omitted in the symbol.

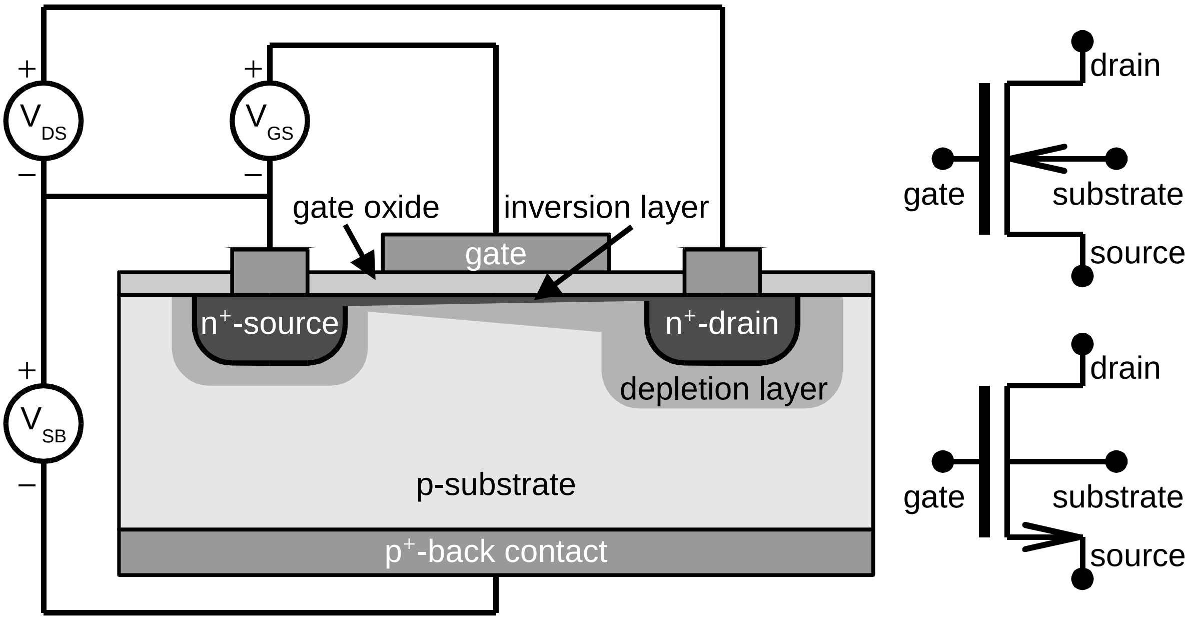

Figure 8.1 Cross-section and two alternative circuit symbols of an n-type metal-oxide-semiconductor field-effect transistor (MOSFET)

A top view of the same MOSFET is shown in Figure 8.2, where the gate length, L, and gate width, W, are identified. Note that the gate length does not equal the physical dimension of the gate, but rather the distance between the source and drain regions underneath the gate. The overlap between the gate and the source and drain region is required to ensure that the inversion layer forms a continuous conducting path between the source and drain region. Typically this overlap is made as small as possible in order to minimise its parasitic capacitance.

The flow of electrons from the source to the drain is controlled by the voltage applied to the gate. A positive voltage applied to the gate, attracts electrons to the interface between the gate dielectric and the semiconductor. These electrons form a conducting channel between the source and the drain, called the inversion layer. No gate current is required to maintain the inversion layer at the interface since the gate oxide blocks any carrier flow. The net result is that the current between drain and source is controlled by the voltage, which is applied to the gate.

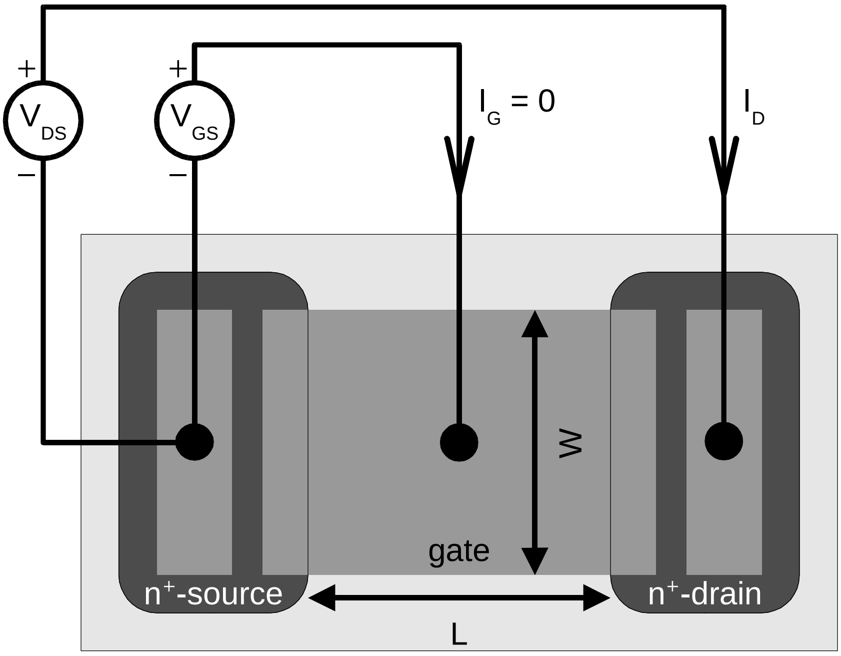

Figure 8.2 Top view of an n-type metal-oxide-semiconductor field-effect transistor (MOSFET)

The typical current versus voltage (I-V) characteristics of a MOSFET are shown in Figure 8.3.

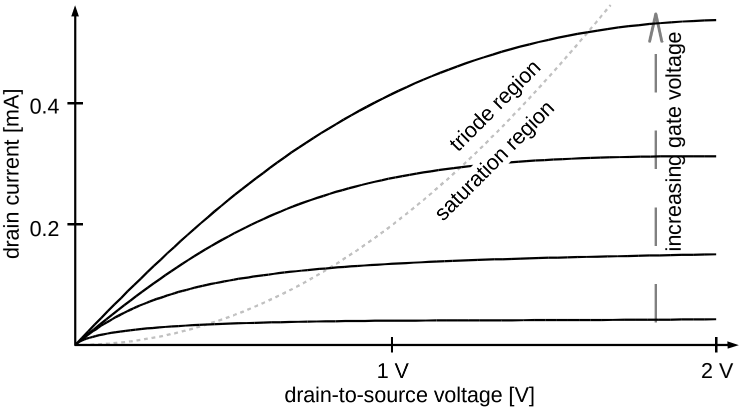

Figure 8.3 I-V characteristics of an n-type MOSFET with V_{GS} = 5 V (top curve), 4 V, 3 V and 2 V (bottom curve)

The effective channel width and effective channel length differ from the drawn dimensions due to mask/etch effects and lateral diffusion. To take these modifications into account, four device process parameters are introduced in SPICE to calculate an effective channel length L_{eff} and an effective channel width W_{eff} respectively.

$$\begin{aligned} W_{eff} &= W_{drawn} + XW - 2\,WD \\ L_{eff} &= L_{drawn} + XL - 2\,LD \end{aligned} \tag{8.1}$$

The mask/etch effect is regarded by *XW* and *XL* respectively. The lateral diffusion is modelled[54] by *WD* and *LD*. For long and broad transistors the effective channel dimensions are approximately the same as the drawn dimensions. In the following the effective channel dimensions are referred to as *W* and *L*.

8.1.1 Summary of the Basic n-MOSFET-Relations

The following relations are derived in [Sze 81], [Sed 98], [Lak 94].

Large Signal Behaviour

While the gate-source voltage V_{GS} is below the threshold voltage V_{thr} no current flows between source and drain. The threshold voltage is given by

$$V_{thr}=2\psi_B+\frac{\sqrt{2\varepsilon_{Si}\,q\,N_A(2\psi_B)}}{C_{ox}} \tag{8.2}$$

with the potential difference ψ_B between the Fermi level and the intrinsic Fermi level, the permittivity of the semiconductor ε_{Si}, the electron charge q, the acceptor doping densities N_A and the insulator capacitance $C_{ox}=\varepsilon_{ox}/d$ per unit area.

In the linear region[55] (triode region), where the drain-source voltage $V_{DS}< V_{GS}-V_{thr}$, the drain current

$$I_D=\beta((V_{GS}-V_{thr})V_{DS}-\frac{V_{DS}^2}{2}) \text{ for } 0\leqslant V_{DS}\leqslant V_{GS}-V_{thr} \tag{8.3}$$

The transconductance parameter β is defined as

$$\beta=KP_n\frac{W}{L} \tag{8.4}$$

with the physical width *W* and the length *L* of the MOSFET, the product KP_n of the charge mobility μ_n and the oxide capacitance per unit area C_{ox}:

$$KP_n=\mu_n C_{ox} \tag{8.5}$$

The oxide capacitance depends on the dielectric constant of the gate oxide ($\varepsilon_{ox}=3.97\cdot 8.85$ aF/µm) and on the oxide thickness t_{ox}.

$$C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}} \tag{8.6}$$

Further increasing of the drain-source voltage results in a saturation of the drain current. Beyond the saturation voltage $V_{DS,sat}=V_{GS}-V_{thr}$ the drain current is ideally independent on V_{DS}:

$$I_D=I_{DS,sat}=\frac{\beta}{2}(V_{GS}-V_{thr})^2 \text{ for } 0\leqslant V_{GS}-V_{thr}\leqslant V_{DS} \tag{8.7}$$

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[54] A detailed overview of MOSFET device modelling is given in [Liu 01]

[55] For $V_{DS}\ll V_{GS}-V_{thr}$ the drain current depends almost linear on V_{DS}.

In fact even in the saturation region a small dependence on V_{DS} is visible due to channel length modulation[56] known as Early[57] effect:

$$I_D=\frac{\beta}{2}(V_{GS}-V_{thr})^2\left(1+\lambda(V_{DS}-V_{DS,sat})\right) \tag{8.8}$$

The channel length modulation parameter depends on the effective transistor length $L_{eff}\approx L$ and the substrate doping N_{bulk} [Cad 93]. An approximation for the modulation parameter is given by:

$$\lambda\approx\frac{1}{L_{eff}}\sqrt{\frac{2\varepsilon_{Si}}{q\,N_{bulk}}\cdot\frac{1}{\mathrm{V}}}\sim\frac{1}{L} \tag{8.9}$$

To receive the correct dimension, the root radicand has to be divided by the unit volt (V).

Small Signal Behaviour

To describe the response of a MOSFET to small signals, a linearisation around the operating point is made. The drain current change with respect to the gate-source voltage for a fixed drain-source voltage is expressed by the transconductance

$$g_m=\frac{\partial I_D}{\partial V_{GS}} \tag{8.10}$$

Therefore the transconductance in the linear region is given by

$$g_m=\beta\,V_{DS} \tag{8.11}$$

In saturation region the transconductance equals

$$g_m=\beta(V_{GS}-V_{thr})\left(1+\lambda(V_{DS}-V_{DS,sat})\right)\overset{\lambda\to 0}{\approx}\sqrt{2\beta I_D} \tag{8.12}$$

The claim for a larger transconductance results in both an increase in width and a higher DC current. In the given process an NMOS with large *W*/*L*-ratio of 100 (60 µm/0.6 µm) and a relatively large DC current of 100 µA results in a transconductance of 1.4 mS. For minimum size transistors the transconductance is in the order of 20 µS.

The output conductance quantifies the drain current variation with a drain-source voltage variation while keeping the gate-source voltage constant:

$$g_{ds}=\frac{\partial I_D}{\partial V_{DS}} \tag{8.13}$$

In the linear region the output conductance decreases with increasing drain-source voltage

$$g_{ds}=\beta(V_{GS}-V_{thr}-V_{DS}) \tag{8.14}$$

---

[56] The effective length of the channel is reduced as the depletion layer width grows with increasing drain voltage (and therefore the reverse-bias drain-bulk voltage is increased).

[57] J. M. Early first described the collector current dependence on the collector voltage in bipolar junction transistors in 1952

and ideally becomes zero, when the device is operated in the saturated region: $g_{ds}=0$. In reality, however, because of the Early effect, the output conductance becomes

$$g_{ds}=\lambda\frac{\beta}{2}(V_{GS}-V_{thr})^2=\lambda I_{DS,sat} \tag{8.15}$$

Remember that λ inversely depends on L (see equation 8.9), it is emphasised that the output conductance decreases with increasing gate length and therefore the output resistance $R_{out}=1/g_{ds}$ is increased. This is important for the realisation of current sources. As a rule of thumb the output conductance (g_{ds}) in the saturation region is two orders[58] of magnitude smaller than the transconductance (g_m):

$$\frac{g_{ds}}{g_m}=\frac{\lambda\frac{\beta}{2}(V_{GS}-V_{thr})^2}{\beta(V_{GS}-V_{thr})\left(1+\lambda(V_{DS}-V_{DS,sat})\right)}\approx\frac{\lambda}{2}(V_{GS}-V_{thr}) \tag{8.16}$$

Body Effect

The threshold voltage of a MOSFET is affected by the voltage, which is applied to the back contact. The voltage difference between the source and the bulk V_{SB} changes the width of the depletion layer and therefore also the voltage across the oxide due to the change of the charge in the depletion region. This results in a shift of the threshold voltage, which equals the difference in charge in the depletion region divided by the oxide capacitance, yielding:

$$V_{thr}=V_{thr0}+\gamma\left(\sqrt{|2\psi_B|+V_{SB}}-\sqrt{|2\psi_B|}\right) \tag{8.17}$$

with the potential difference ψ_B between the Fermi level and the intrinsic Fermi level. The threshold V_{thr0} at $V_{SB}=0$ V was defined in equation 8.2. The body factor γ is defined as

$$\gamma=\frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{ox}} \tag{8.18}$$

with the electron charge q, the permittivity of the semiconductor ε_{Si}, the acceptor doping densities N_A and the insulator capacitance C_{ox} per unit area.

As one can see in Figure 8.1 the bulk contact acts as a gate of a junction field effect transistor (JFET) between source and drain. Variation of the bulk voltage with respect to the source results in a current change. Therefore the body transconductance g_{mb} is defined:

$$g_{mb}=\frac{dI_D}{dV_{BS}} \tag{8.19}$$

Using equations 8.7, 8.17, 8.12 this yields $g_{mb}=\chi\cdot g_m$ with

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[58] The shorter the channel length the larger the channel length modulation. Unfortunately in deep submicron technologies the output conductance cannot be made a hundred times smaller than the transconductance.

$$\chi=\frac{dV_{thr}}{dV_{SB}}=\frac{\gamma}{2\sqrt{|2\psi_B|+V_{SB}}} \tag{8.20}$$

Typically the value of χ lies in the range of 0.1 to 0.3.

Typical Process Parameters

The following table (Table 8.1) gives an overview of typical values of process parameters:

parameter name	symbol	typical values for NMOS (PMOS)	units
gain factor	KP_n (KP_p)	120 (40)	$\mu A/V^2$
gate-oxide thickness	t_{ox}	12.5	nm
channel-length modulation	λ	0.01...0.1	V^{-1}
effective surface mobility	μ_n (μ_p)	430 (145)	cm^2/Vs
effective substrate doping	N_{subN} (N_{subP})	145 (52)	$10^{15}/cm^3$
threshold voltage	V_{thrN} (V_{thrP})	720...850 (−800...850) (depending on channel length)	mV
body factor (long channel L=10 µm)	γ_n (γ_p)	0.8 (0.48)	$V^{1/2}$
oxide capacitance	C_{ox}	2.76	$fF/\mu m^2$
mask/etch effect on *W*	XW	0.0 (0.0)	nm
mask/etch effect on *L*	XL	0.0 (0.0)	nm
lateral bulk diffusion along width	WD	−8.94 (38.78)	nm
lateral diffusion	LD	144.9 (99.28)	nm
flicker noise coefficient (see section 8.4.2)	K_f'	0.6896 (1.126)	10^{-26} C^2/m^2
flicker noise exponent	af	1.343 (1.772)	–
flicker noise frequency exponent	ef	1.0	–
poly sheet resistance		33	$\Omega/\square$

Table 8.1 Typical process and simulation parameters

Subthreshold Region (Weak Inversion)

When the gate-source voltage is below the threshold voltage and the semiconductor surface is in weak inversion, the transistor works in the subthreshold region. It is particularly important for low-voltage, low-power applications and special purpose applications respectively. A model for transistors operating in the subthreshold region is given by [Vit 77]:

$$I_D = \frac{W}{L} I_{DO} \exp\left(\frac{q\,V_G}{n\,k\,T}\right)\left[\exp\left(\frac{-q\,V_S}{k\,T}\right) - \exp\left(\frac{-q\,V_D}{k\,T}\right)\right] \tag{8.21}$$

The subthreshold slope factor n ($\approx$1) and I_{DO} are process-dependent parameters. I_{DO} depends on the source-bulk voltage V_{SB} and on the threshold voltage V_{thr}. For the saturation region ($V_{DS} > 3kT/q$), $V_S = 0$ and $qV_D \gg kT$ equation 8.21 simplifies to:

$$I_D \approx \frac{W}{L} I_{DO} \exp\left(\frac{q\,V_{GS}}{n\,k\,T}\right) \tag{8.22}$$

Unfortunately, this equation fails to model the transistor in the transition from weak to strong inversion. The transition region is called the moderate inversion region. A complete treatment of the operation of the transistor through this region is given in [Tsi 82] and [Ant 82].

For the sake of completeness the transconductance in weak inversion is just given:

$$g_m \approx \frac{q}{n\,k\,T} I_D \tag{8.23}$$

It should be annotated that a very high transconductance can be realised operating a transistor in weak inversion: For a current of 10 µA the transconductance at room temperature is 400 µS.

8.2 Latch-Up

A by-product of the bulk[59] CMOS structure is a pair of parasitic bipolar junction transistors (BJT) as exemplarily shown for an inverter configuration in Figure 8.4. The collector of each BJT is connected to the base of the other transistor in a positive feedback structure. A phenomenon called latch-up can occur when both BJT's conduct, creating a low resistance path between V_{DD} and *GND*, and the product of the gains of the two transistors in the feedback loop, $A_1 \times A_2$, is greater than one. The result of latch-up is at the minimum a circuit malfunction, and in the worst case, the destruction of the device.

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[59] In a bulk CMOS structure one type of transistors is realised in the substrate: All bulks are intrinsically connected. The complementary transistor type is realised in dedicated wells.

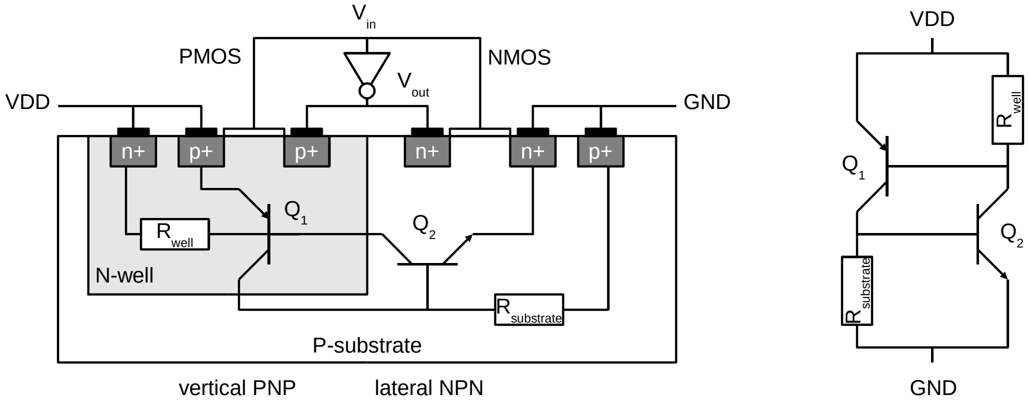

Figure 8.4 Cross section of parasitic transistors in bulk CMOS and equivalent circuit

Latch-up may begin when the base of Q_1 (N-well) drops below V_{DD} due to a noise spike or an improper circuit hook-up. If sufficient current flows through $R_{substrate}$ to turn on Q_2 $(I\cdot R_{substrate}>0.7\ \text{V})$, this will draw current through R_{well}. If the voltage drop across R_{well} is high enough, Q_1 will stay turned on, and a self-sustaining low resistance path between the power rails is formed[60]. If the gains are such that $A_1 \times A_2 > 1$, latch-up may occur. Once latch-up has begun, the only way to stop it is to reduce the current below a critical level, usually by removing power from the circuit.

The most likely place for latch-up to occur is in pad drivers, where large voltage transients (the wire bonds form an inductive load; switching these loads causes voltage spikes exceeding the power supply voltage) and large currents are present.

8.2.1 Preventing Latch-Up

Fabrication/Design Approaches

1. Reduce the gain product $A_1 \times A_2$
    - move n-well and n^+-source/drain farther apart increases length of the base of Q_2 and reduces gain β; as a drawback it also reduces CMOS circuit density
    - buried n^+ layer in well reduces gain of Q_1
2. Reduce the well and substrate resistances, producing lower voltage drops
    - higher substrate doping level reduces $R_{substrate}$
    - reduce R_{well} $(R_{substrate})$ by making low resistance contact to V_{DD} (GND)
    - guard rings around p- and/or n-well with frequent contacts to the rings reduce the parasitic resistances
3. Implementation of CMOS technology in silicon on insulator (SOI) substrates is an ultimate solution to the CMOS latch-up: Both transistor polarities are separated by insulating trenches.

---

[60] The npnp-structure in the circuit is comparable to a thyristor or SCR (silicon controlled rectifier).

Systems Approaches

Make sure power supplies are off before plugging into a board. A "hot plug in" of an unpowered circuit board or module may cause signal pins to see surge voltages greater than 0.7 V higher than V_{DD}, which rises more slowly to its peak value. When the chip comes up to full power, sections of it could be latched.

Carefully enclose electrostatic protection devices associated with I/O pads with guard rings. Electrostatic discharge (ESD) can trigger latch-up. ESD enters the circuit through an I/O pad, where it is clamped to one of the rails by the ESD protection circuit. Devices in the protection circuit can inject minority carriers in the substrate or well, potentially triggering latch-up.

Radiation, including X-rays, cosmic, or alpha rays, can generate electron-hole pairs as they penetrate the chip. These carriers can contribute to well or substrate currents.

Sudden transients on the power or ground bus, which may occur if large numbers of transistors switch simultaneously (e. g. in shift registers), can drive the circuit into latch-up.

8.3 Basic Circuits

8.3.1 A review of important circuits

A feedback capacitor between the inverting output and the input of an amplifier increases the effective input capacitance C_{in}. The amplification of the amplifier is given by $A = dU_{out}/dU_{in}$ (see Figure 8.5).

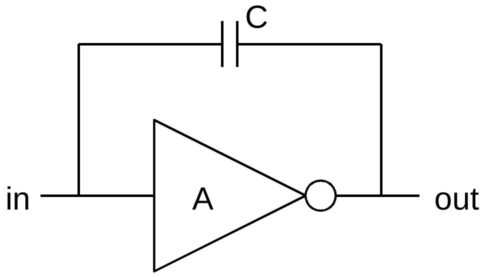

Figure 8.5 Arrangement to calculate the effective input capacitance of an inverting amplifier

A charge dQ deposited at the input gives a rise in input voltage of

$$dU_{in} = dQ / C_{in} \tag{8.24}$$

As a result the output of the inverting amplifier changes: $dU_{out} = A \cdot dU_{in}$. Assuming an ideal amplifier with no input capacitance the charge dQ completely flows to the feedback capacitor C:

$$dQ = C(dU_{in} - dU_{out}) = C\, dU_{in}(1 - A) \tag{8.25}$$

Comparing 8.24 with 8.25 the input capacitance is given by

$$C_{in}=C(1-A) \tag{8.26}$$

Remembering that the amplification of an inverting amplifier is negative, the effective input capacitance is *1+|A|* times larger than the real feedback capacitor *C*.

Capacitive voltage divider

Figure 8.6 shows a capacitive voltage divider. The output voltage is calculated to be:

$$U_{out}=U_{in}\frac{Z_2}{Z_1+Z_2}=U_{in}\frac{\frac{1}{i\omega C_2}}{\frac{1}{i\omega C_1}+\frac{1}{i\omega C_2}}=U_{in}\frac{C_1}{C_1+C_2} \tag{8.27}$$

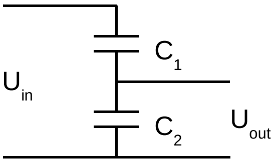

Figure 8.6 Capacitive voltage divider

8.3.2 Current Mirrors

In integrated circuits a reference current, a fractional amount of a current or a multiple often has to be replicated. To realise such a current mirror, the characteristics of a MOSFETs can be exploited.

Basic Current Mirror

A current creates a current dependent voltage drop on a diode connected transistor (drain and gate connected). The current versus voltage characteristic

$$I=\frac{\beta}{2}(V-V_{thr})^2 \text{ for } V>V_{thr} \tag{8.28}$$

looks similar to a diode, which is a more than linear rise in current above a certain threshold with increasing voltage. This voltage is used as gate voltage of a similar transistor. By holding this transistor in saturation $(V_{out}=V_{DS}\geq V_{GS}-V_{thr})$ its output current is ideally the same as the reference current $(I_{out}=I_{ref})$.

Due to Early effect the current mirror has a finite output resistance, resulting in a voltage dependent output current. The output resistance is simply the inverse of the output conductance:

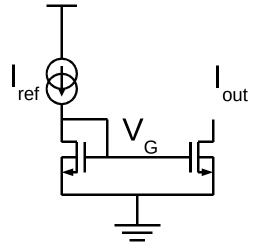

Figure 8.7 Basic current mirror

$$r_{out} = \frac{1}{g_{ds}} \tag{8.29}$$

For long and small transistors it can be as large as 1 MΩ. To even increase this output resistance, more sophisticated mirrors must be used, e. g. a cascoded or regulated current mirror (see below). Owing to the relatively large small signal output resistance current mirrors are widely-used as active load resistance in all kind of analog circuits, e. g. amplifiers (see below).

An arbitrary fraction or, more frequent, a multiple of a current is achieved by an appropriate ratio of the W/L ratioes. The matching between the reference current and the target multiple of the reference current is a main issue of current mirrors. To achieve good matching, usually the length is kept the same. To realise a whole-numbered multiple, it is better for precision to copy the corresponding number of transistors than to enlarge its width to overcome several edge effects. A good matching requires the same physical orientation and current direction of both transistors. Other layout methods can be used to minimise the first-order effects of variations of process parameters such as gate-oxide thickness, lateral diffusion, oxide encroachment and oxide charge density. [Bak 97].

To evaluate the influence of the threshold voltage variation in a 1:1-current mirror, the threshold voltages are assumed to be $V_{thr1,2} = V_{thr} \pm \frac{1}{2}\Delta V_{thr}$. This leads to

$$\frac{I_{out}}{I_{ref}} = \frac{\beta\left(V_{GS} - V_{thr} - \frac{1}{2}\Delta V_{thr}\right)^2}{\beta\left(V_{GS} - V_{thr} + \frac{1}{2}\Delta V_{thr}\right)^2} \approx 1 - \frac{2\Delta V_{thr}}{V_{GS} - V_{thr}} \tag{8.30}$$

A larger gate-source voltage V_{GS} reduces the influence of the threshold voltage mismatch ΔV_{thr}. For a given current V_{GS} is increased by using longer devices.

The same analysis is performed on the transconductance parameter KP:

$$\frac{I_{out}}{I_{ref}} \approx 1 + \frac{\Delta KP}{KP} \tag{8.31}$$

For good matching one have to use long devices and keep both transistors in the current mirror as close as possible, as the local process parameter variation is smaller than for larger distances.

Another issue is the noise output of a current mirror. To calculate the total output noise, the transistors' noise is represented by noise current sources shown in Figure 8.8.

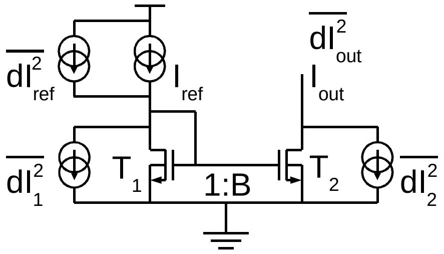

Figure 8.8 Noise in a single MOSFET current mirror

The noise generated by the reference current source I_{ref} is denoted by di^2_{ref}. The current ratio B designates the ratio between the output current and the reference current by the geometry of the transistors. The total output noise is then given by

$$di^2_{out}=(di^2_{ref}+di^2_1)B^2+di^2_2 \tag{8.32}$$

Substitution of the transistor noise current generators by (see equation 8.58)

$$di^2=\frac{8}{3}k\,T\,g_m\,df \tag{8.33}$$

yields to

$$\begin{aligned} di^2_{out}&=B^2\,di^2_{ref}+\frac{8k\,T}{3}(B+1)\,g_{m2}\,df \\ &=B^2\,di^2_{ref}+\frac{8k\,T}{3}(B+1)\sqrt{2\,KN\frac{W_2}{L_2}I_{out}}\,df \end{aligned} \tag{8.34}$$

For a given output current, the noise output current becomes smaller if B and W/L are smaller. The smaller W/L the larger V_{GS} must be, which on the one hand causes a large output compliance voltage, but on the other hand a large V_{GS} improves matching.

Cascode Current Mirror

To enhance particularly the output impedance, a cascode[61] is used to stabilise the drain voltage of the output transistor to reduce the influence of the Early effect.

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[61] Historically cascode stands for casc̲a̲d̲e of a common cath̲o̲d̲e̲ and a common grid tube stage. In CMOS it translates to a cascade of a common source and a common gate stage.

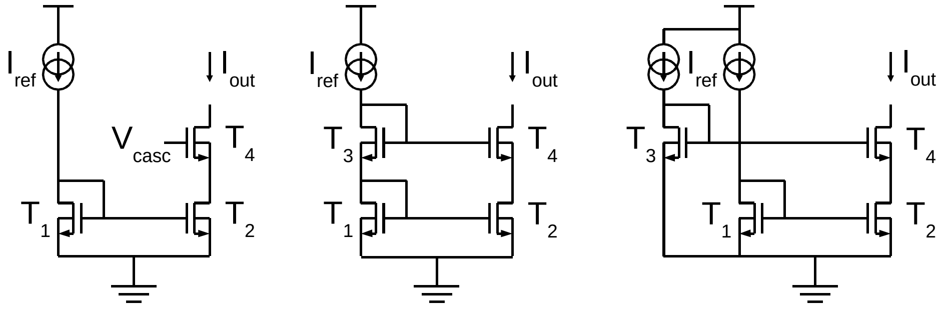

Figure 8.9 Cascode current mirror and two practical realisations

To calculate the small signal output resistance of the cascode current mirror shown in Figure 8.9, the current change dI_{out} of the output due to a voltage change dU_{out} has to be determined. With the output current change dI_{out} the drain-source voltage of T_4 changes $(dU_{DS4}=dI_{out}/g_{ds4})$ as well as the drain-source voltage of T_2 $(dU_{DS2}=dI_{out}/g_{ds2})$. For a fixed voltage V_{casc} the latter results in a gate-source voltage change of $dU_{GS4}=-dU_{DS2}$.

Solving the output current change

$$dI_{out}=-g_{m4}dU_{DS2}+g_{ds4}(dU_{out}-dU_{DS2})=-\frac{g_{m4}}{g_{ds2}}dI_{out}+g_{ds4}dU_{out}-\frac{g_{ds4}}{g_{ds2}}dI_{out} \tag{8.35}$$

for $r_{out}=dU_{out}/dI_{out}$ yields:

$$r_{out}=\frac{dU_{out}}{dI_{out}}=\frac{1}{g_{ds4}}\left(1+\frac{g_{m4}}{g_{ds2}}+\frac{g_{ds4}}{g_{ds2}}\right)\approx\frac{g_{m4}}{g_{ds4}g_{ds2}} \tag{8.36}$$

As stated before g_{m4}/g_{ds4} can be as large as 100, which enhances the output resistance compared to the basic current mirror just by this factor.

Two practical realisations of the cascode current mirror are shown in Figure 8.9. In the first realisation a diode connected transistor T_3 produces the necessary voltage drop to keep the output transistor T_2 via the source follower T_4 in saturation. In this case the output voltage is limited to keep all transistors in saturation to realise a nearly voltage independent current:

$$V_{out}\geqslant V_{thr}+2\sqrt{\frac{2I}{\beta}} \tag{8.37}$$

This minimal voltage is reduced by the second realisation: T_2 is in saturation, if

$$V_{DS2}\geqslant V_{GS2}-V_{thr}=\sqrt{\frac{2I}{\beta_2}} \tag{8.38}$$

Therefore the gate-source voltage of T_3 has to exceed the gate-source voltage by V_{DS2}. Assuming $\beta_1=\beta_2=\beta_4$:

$$V_{GS3}-V_{thr}=\sqrt{\frac{2I}{\beta_3}}=\sqrt{\frac{2I}{\beta_2}}+\sqrt{\frac{2I}{\beta_4}}=2\sqrt{\frac{2I}{\beta_4}} \tag{8.39}$$

This results in $4\beta_3=\beta_4$. Either T_3 is made at least four times longer than T_4 or the current through T_3 is set to four times the reference current.

The minimal voltage at the output in the second realisation is reduced by the threshold voltage V_{thr} compared to the first realisation.

Feedback Current Mirror

The basic current mirror can also be improved significantly with negative feedback [Bak 97]. There are two widely used current mirrors of this type, known as Wilson current mirror and the regulated cascode current mirror.

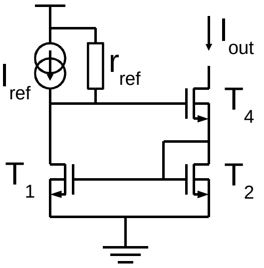

Figure 8.10 Wilson current mirror

The output resistance is approximated by [Bak 97]

$$r_{out} \approx r_{ds4}\left[1+g_{m1}\left(r_{ref}\|r_{ds1}\right)+\frac{g_{mb4}}{g_{m2}}+\frac{g_{ds4}}{g_{m2}}\right] \approx r_{ds4}\left(1+g_{m1}\frac{r_{ds4}}{2}\right) \text{ for } r_{ds4}\approx r_{ref}\approx r_{ds1} \tag{8.40}$$

The Wilson current mirror has a similar output resistance as the cascode current mirror.

Regulated Cascode Current Mirror

The regulated cascode current mirror uses a cascode transistor, whose gate voltage is regulated to compensate the current change due to Early effect in the common source transistor T_3 (see Figure 8.11).

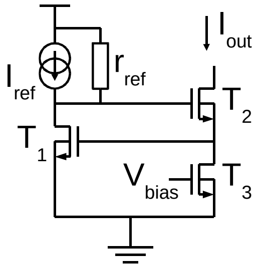

Figure 8.11 Regulated cascode current sink

The output resistance is derived in [Bak 97]

$$r_{out}=r_{ds4}\left[1+g_{m4}r_{ds2}\left(1+g_{m1}\left(r_{ref}\|r_{ds1}\right)\right)+\frac{g_{mb4}}{g_{ds2}}+\frac{g_{ds4}}{g_{ds2}}\right] \approx g_{m1}g_{m4}\left(r_{ref}\|r_{ds1}\right)r_{ds2}r_{ds4} \tag{8.41}$$

and can be extended to a factor of 10000 over the basic current mirror.

8.3.3 Amplifiers

There are three possible ways to realise a four terminal device (two terminals as input, two terminals as output) based on a single three[62] terminal device such as the MOSFET, depending on which MOSFET-terminal has both an input and output connection.

Common Source Amplifier

In the common source amplifier the input voltage is applied between gate and source whereas the output voltage is tapped between drain and source. So both the input and the output are connected to the source in common as shown in Figure 8.12.

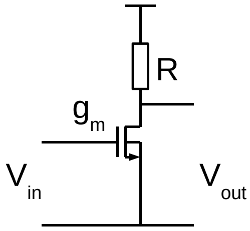

Figure 8.12 Common Source Amplifier

If the DC-conditions are properly chosen (the DC-input voltage exceeds the threshold voltage resulting in a current through the transistor, causing a voltage drop across the resistor small enough to keep the transistor in saturation), the small signal voltage amplification $A=dV_{out}/dV_{in}$ is calculated: The current change dI_{out} in the transistor due to an input voltage change dV_{in} is given by

$$dI_{out}=g_m\,dV_{in} \tag{8.42}$$

The current change causes a voltage change across the resistor:

$$dV_{out}=-R\,dI_{out} \tag{8.43}$$

Therefore the small signal voltage amplification is given by

$$A=\frac{dV_{out}}{dV_{in}}=-R\,g_m \tag{8.44}$$

To satisfy the demand for a large voltage amplification, both the transconductance (large W/L, high DC-bias current) and the load resistance must be maximised. A large resistor in combination with a high current leads to a large voltage drop. Beside

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[62] Assuming that the bulk contact is connected to source or to a fixed voltage reduces the MOSFET to a three terminal device.

the voltage limitation by the power supply this would cause a high power dissipation, which is a serious problem in VLSI[63]-design. To overcome this problem, the output resistance of a real current source (e. g. current mirror) is used as an active load. It offers a large small signal resistance while producing a relatively small voltage drop due to the DC-bias current.

The common source input impedance is only capacitive. For low frequencies the impedance is therefore quite high and the common source amplifier can be used as a voltage amplifier for all kind of voltage sources.

Now the frequency response of the common source will be studied. In Figure 8.13 the equivalent schematic is explicitly drawn. The output resistance R_s of the signal source forms a low-pass filter together with the gate-drain capacitance C_{gd} and the gate-source capacitance C_{gs}. For simplicity the gate-bulk capacitance is neglected[64]. As the common source amplifier is inverting (a positive input signal causes a negative output signal) the capacitance seen at the input[65] is given by $C_{in}=C_{gs}+C_{gd}(1+|A|)$ (see section 8.3.1). Therefore an input time constant of

$$\tau_{in}=\frac{1}{\omega_{in}}=R_s(C_{gs}+C_{gd}(1+|A|)) \tag{8.45}$$

is obtained.

Another low-pass filter is formed by the load resistor R_{load} (including an additional load resistance of the subsequently connected circuit and the output resistance of the transistor) and the load capacitance C_{load}, consisting of the capacitance of the load resistance, a load capacitance of the next stage and the drain-bulk capacitance of the transistor.

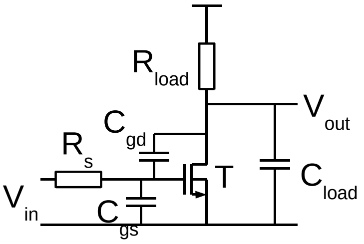

Figure 8.13 Equivalent schematic of the common source amplifier with intrinsic capacitances

The output capacitance is given by $C_{out}=C_{load}+C_{gd}(1+1/|A|)$, resulting in an output time constant

$$\tau_{out}=\frac{1}{\omega_{out}}=R_{load}(C_{load}+C_{gd}(1+\frac{1}{|A|})) \tag{8.46}$$

---

[63] Very Large Scale Integration

[64] Later the gate-bulk capacitance can simply be added to the gate-source capacitance.

[65] As the gate-drain capacitance C_{gd} is obviously dominating the input capacitance and, as a consequence, is limiting the bandwidth, it is often referred to as Miller-effect [Hor 89].

The frequency response of this amplifier is given by the product of the transfer functions of two low-pass filters [Bak 98]:

$$A(s) = \frac{-g_m R_{load}}{\left(1+\frac{s}{\omega_{in}}\right)\left(1+\frac{s}{\omega_{out}}\right)} \tag{8.47}$$

Assuming a low input resistance R_s the cut-off-frequency is given by

$$\omega_{-3dB} = \frac{1}{R_{load} C_{Leq}} \tag{8.48}$$

The equivalent output load C_{Leq} is approximated by $C_{Leq} = C_{load} + C_{gd}$.

If otherwise the input resistance R_s is large, the dominant pole in equation 8.47 is given by the input time constant. A relatively large voltage amplification results in a significant reduction of bandwidth due to the apparently large input capacitance. (Miller-effect). The cut-off-frequency is then given by

$$\omega_{-3dB} = \frac{1}{R_s(C_{gs} + C_{gd}(1+|A|))} \tag{8.49}$$

In the large signal behaviour the common source amplifier loses its linearity as the transconductance changes due to a different operation point. Most of the mentioned drawbacks can be overcome by different amplification topologies or by means of feedback.

Common Drain Amplifier (Source follower)

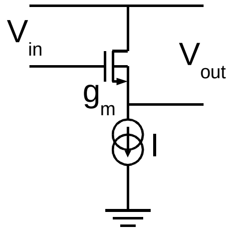

Figure 8.14 Common drain amplifier

In the common drain amplifier the input and output have the drain of the transistor drawn in Figure 8.14 in common. The gate-source voltage drop depends only on the bias current I (see equation 8.9) as long as the transistor is operated in saturation. For the reason that the output voltage follows directly the input signal this configuration is also called source follower. The small signal voltage gain is unity. The large signal voltage gain (for low frequencies) is practically reduced by the body effect (bulk and source cannot be connected in each technology) and the finite resistance of the current source. As the output is in phase with the input signal, the gate-source capacitance plays no roll. Therefore this amplifier has a very large bandwidth. It is usually used as an impedance converter due to its high input impedance.

Common Gate Amplifier

The common gate amplifier uses the source with respect to the gate as the input. Therefore it has a very low input impedance of $(1/g_m)$. It is used to convert the signal from a current source to a voltage. The input current signal produces an output signal of $dU_{out}=R\cdot dI_{in}$. As the input and output signals are in phase, the Miller capacitance does not significantly limit the bandwidth.

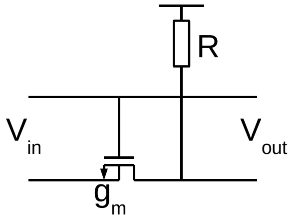

Figure 8.15 Common gate amplifier

(Straight) Cascode Amplifier

In the common source amplifier the bandwidth is limited by the Miller capacitance. To overcome this problem, a cascaded stage of a common source and a common gate amplifier is used as shown in Figure 8.16.

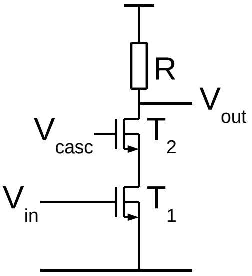

Figure 8.16 Straight cascode amplifier

The common gate stage (T_2) forces the drain of the common source stage (T_1) to be held at a more or less fixed voltage (related to V_{casc}=const) as the input impedance of the common gate stage is relatively low $(1/g_{m2})$ and therefore the current change $(dI_1=g_{m1}\cdot dV_{in})$ results in a small voltage change:

$$dV_{ds1}\approx\frac{g_{m1}}{g_{m2}}dV_{in} \tag{8.50}$$

As the output voltage swing of the first stage (T_1) is relatively small compared to the output voltage swing of a simple common source amplifier the negative feedback via the Miller capacitance is reduced as well. The output current of T_1 passes T_2 and produces a voltage drop across the resistor R. Since the current change is given by g_{m1} the voltage amplification of the cascode amplifier is the same as of the common source amplifier $(A=-g_{m1}\cdot R)$ but it has a broader bandwidth.

As pointed out in equation 8.12, the transconductance depends on the DC-bias current. To realise a large voltage gain, both the load resistor and the current should be large, which has two drawbacks: Firstly, the output voltage swing is limited as both transistors T_1 and T_2 must be kept in saturation. The relatively large current also creates a relatively large voltage drop across the resistor, which can be overcome to a certain extent by the use of an active load (real current source with high output impedance). Secondly the high current through all three devices (T_1, T_2, R) causes a high power consumption as the voltage drop across all three components has to be large to achieve a given output voltage swing.

These disadvantages are reduced either by the use of an improved straight cascode, shown in Figure 8.17, or by the realisation as a folded cascode amplifier, described in the next paragraph.

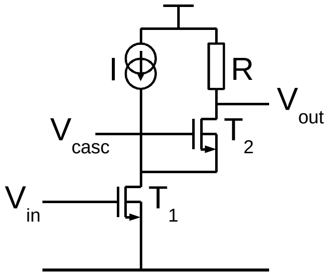

Figure 8.17 Improved straight cascode amplifier

Folded Cascode Amplifier

The operating principle of the folded cascode is similar to the straight cascode. The drain voltage of the input transistor is held to a stable voltage by means of a common gate stage. In the folded cascode this stage is turned down as shown in Figure 8.18 by the use of a complementary transistor. Therefore only a small amount of the DC-bias current I flows through the cascode transistor and the load resistance. The great part of the DC-bias current is used to realise a large transconductance in the input transistor. A current change in the input transistor implicates a complementary current change in the output branch. The voltage gain is $A = -g_{m1} \cdot R$.

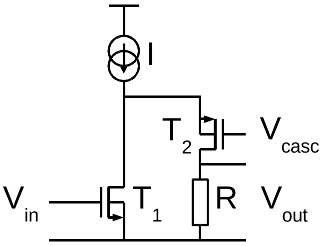

Figure 8.18 Folded cascode amplifier

As the bigger part of the current flows only in the current source and in the input transistor the power consumption can be kept low as the output voltage swing is not determined by the voltage drop across the input transistor and the current source and therefore could be kept small.

Regulated Cascode Amplifier

The drain voltage of the input transistor is not really fixed by the cascode transistor. As the load seen by the input transistor is $1/g_{m2}$ of the cascode transistor, the voltage swing at the drain due to an input signal is given by equation 8.50.

To reduce the drain voltage swing of the input transistor even more than with a fixed cascode transistor, a regulated cascode is used: The drain voltage of the input transistor is monitored and controls the gate voltage of the cascode transistor as shown in Figure 8.19. The influence of the Miller capacitance is not only reduced to increase the bandwidth, but also to reduce the input capacitance of the first stage, which will be exploited in the charge sensitive amplifier.

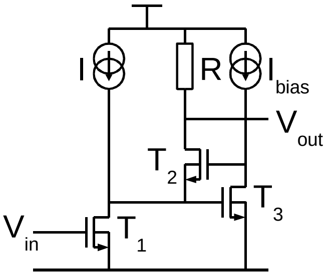

Figure 8.19 Regulated cascode amplifier

The input resistance of the cascode branch (looking into the source of T_2) is given by:

$$r_{reg} = \frac{-dV_{gs3}}{dI_2} \approx \frac{1}{g_{m2}(1+g_{m3}\, r_{load3})} \approx \frac{1}{g_{m2} A_3} \tag{8.51}$$

Here, the load resistance r_{load3} seen by T_3 and the voltage gain of the common source amplifier T_3 are used. The input resistance of the cascode transistor T_2 is therefore reduced by the voltage gain of T_3.

Differential Stage

The differential amplifier is the most widely used circuit building block in analog integrated circuits. Its principle is given in Figure 8.20.

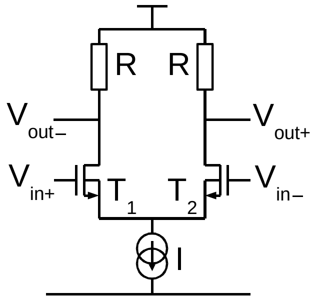

Figure 8.20 Principle of a differential stage

To calculate the small signal voltage gain of this stage, the following assumptions are made: The differential stage is properly DC-biased, i. e. the transistors T_1 and T_2 are operated in saturation. Both transistors are assumed to be exactly the same and the input voltage $V_{in+}=V_{in-}$. Applying a small voltage dV_{in} so that $V_{in+}=V_{in+}+dV_{in}/2$ and $V_{in-}=V_{in-}-dV_{in}/2$, results in a current change through T_1 of $dI_1=g_{m1}\cdot dV_{in}/2$ and in T_2 of $dI_2=-g_{m2}\cdot dV_{in}/2$.

The output voltage change $dV_{out}=dV_{out+}-dV_{out-}=-(R\cdot dI_2-R\cdot dI_1)=R\cdot g_m\cdot dV_{in}$ with $g_m=g_{m1}=g_{m2}$. The small signal amplification is therefore $A=R\cdot g_m$.

For the same reasons as in the basic amplification circuits resistors are avoided[66]. A practical realisation is shown in Figure 8.21 [Sed 98]. The currents $dI_1=g_{m1}\cdot dV_{in}/2$ and $dI_2=-g_{m2}\cdot dV_{in}/2$ are as above. As dI_1 is mirrored via T_3 and T_4 the total output current $dI_{out}=dI_1-dI_2=g_m\cdot dV_{in}$. The output resistance is given by $r_o=r_{ds4}||r_{ds2}$. For modern technologies, a gain of 20 to 100 is achievable. To obtain higher gains, a cascode current mirror and a cascoded differential stage or a multi-stage amplifier can be used. As the differential amplifier provides an output current, which is converted to an output voltage by the output resistance, depending on the applied input voltage it is often referred to as operational transconductance amplifier (OTA).

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[66] As long as large voltage amplification is needed, resistors are avoided. For low amplification (in the order of two) and large bandwidth (high speed application) resistors are still used.

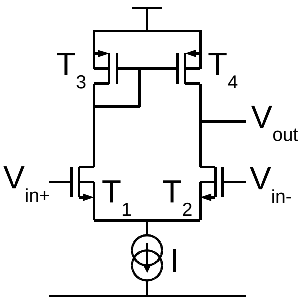

Figure 8.21 An active-loaded differential amplifier

The shown OTA has a poor output range, which is given by the condition that T_2 and T_4 must be kept in saturation. An improved symmetrical CMOS OTA is shown in Figure 8.22, which has an output voltage range between ground and the supply voltage. A detailed description is given in [Lak 94].

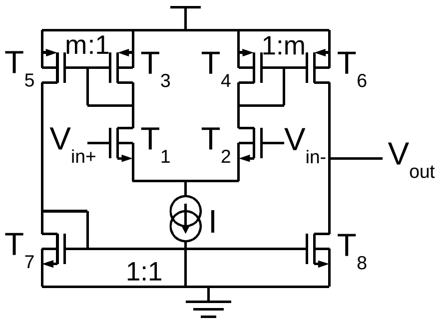

Figure 8.22 Symmetrical OTA

One important aspect of differential amplifiers is the dependence of the performance on the matching of devices. Layout techniques can be used to minimise the first-order effects of mismatch due to gradients in oxide thickness, doping concentration and other process variations [Bak 98]. An important issue is the input offset voltage resulting from mismatches in threshold variation, geometry and load resistances. The offset voltage is defined as the voltage at the input, which must be applied to get no voltage at the output $(R_1 \cdot I_1 = R_2 \cdot I_2)$. In the differential stage of Figure 8.20 the input offset voltage is evaluated to be

$$\begin{aligned} V_{offset} &= V_{gs1} - V_{gs2} = V_{thr1} + \sqrt{\frac{2I_1}{\beta_1}} - V_{thr2} - \sqrt{\frac{2I_2}{\beta_2}} \\ &= \Delta V_{thr} - \frac{V_{gs} - V_{thr}}{2}\left(\frac{\Delta R_{load}}{R_{load}} + \frac{\Delta(W/L)}{(W/L)}\right) \end{aligned} \tag{8.52}$$

In the last term the mean values $V_{gs}=(V_{gs1}+V_{gs2})/2$, $V_{thr}=(V_{thr1}+V_{thr2})/2$, $R_{load}=(R_1+R_2)/2$ and $W/L=(W_1/L_1+W_2/L_2)/2$ and the differences $\Delta V_{gs}=V_{gs1}-V_{gs2}$, $\Delta V_{thr}=V_{thr1}-V_{thr2}$, $\Delta R_{load}=R_1-R_2$ and $\Delta(W/L)=W_1/L_1-W_2/L_2$ are used. Mismatches resulting from differences in the load resistance and unequal geometry can be reduced by designing with a small V_{gs} close to V_{thr} (short L, broad W).

Cascoded Differential Stage

The gain bandwidth product *(GBW)* as well as the power supply rejection ratio (PSRR) of the previous OTA are improved by a folded cascode design as shown in Figure 8.23. The drain voltages of the input transistors are cascoded by T_6 and T_7. The current ratio through T_1 and T_2 depends on the input voltage difference. Twice the current difference is provided at the output [Bak 98], [Lak 94].

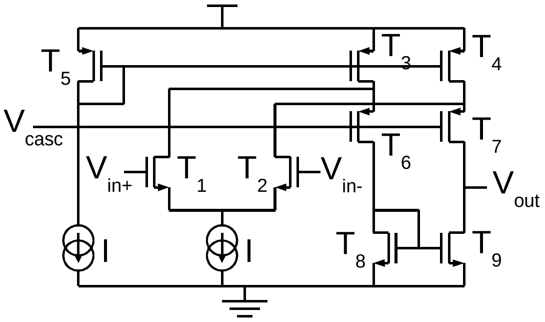

Figure 8.23 Folded cascode OTA

The maximum input voltage is limited by the condition that $T_{1,\,2}$ and $T_{3,\,4}$ are kept in saturation. If an adequate cascode voltage V_{casc} is chosen, the upper input voltage limit can be extended to the power supply voltage. The lower input voltage range is given by the requirement that $T_{1,\,2}$ and their bias current source are in saturation, resulting in a lower limit, which is higher than the threshold voltage (V_{thrN}). A complementary input stage would cover the input voltage range down to ground.

Output Stage

In many applications, an OTA must drive a resistive or capacitive load. In this situation, a buffer between the OTA and the load is used to ensure that the gain of the OTA is not degraded. Figure 8.24 shows an example of an output buffer that employs source followers. The source follower T_2 is biased by T_1 to keep both output transistors $(T_3,\ T_4)$ on: $V_{SG2} > V_{thrP} + V_{thrN}$. The gain through this buffer is approximately unity. The main drawback of this configuration is the limited output swing. The maximum output voltage is less than $V_{DD} - V_{thrN}$ (with body effect), while the minimum output voltage is V_{thrP}.

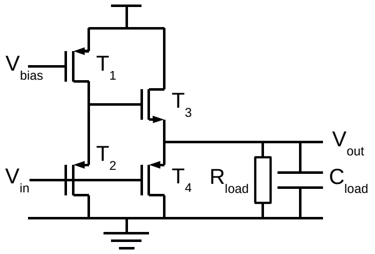

Figure 8.24 Unity gain output buffer

The advantage of the second example, shown in Figure 8.25, is the capability of the output to approach the supply voltages (rail-to-rail). This is achieved by using two complementary common source amplifiers $(T_3,\ T_4)$. As this arrangement provides additional gain, a frequency compensation capacitor C_{comp} is added. The diode connected transistors T_5, T_6 can be thought of zero-cancelling resistors $(R_z=1/g_{m5}\ ||\ g_{m6})$. The transistors T_1, T_2 are the output stage transistors of the OTA.

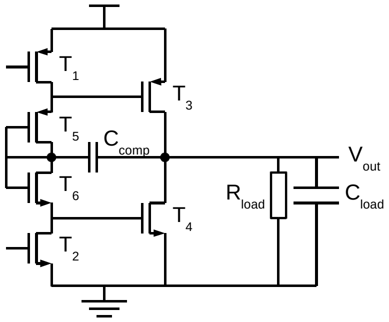

Figure 8.25 Output buffer with gain and full output swing

In some cases the pole zero cancelation resistors are not needed, yielding to a configuration as shown in Figure 8.26.

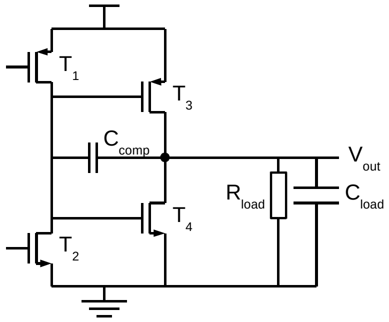

Figure 8.26 Reduced output buffer

The output stage now consists of a simple inverter. To calculate the maximum quiescent current (no load connected), the output is connected to the input of the inverter (two complementary diode connected transistors). The current through both saturated transistors *(T_3, T_4)* is equal. Assuming that both transistors are designed to have the same transconductance parameter ($\beta=\beta_P=\beta_N$) and that the absolute value of the threshold voltages are equal *($V_{thr}=V_{thrN}=-V_{thrP}$)*, the maximal quiescent current is calculated to be

$$I=\frac{\beta}{8}(V_{DD}-2\,V_{thr})^2 \tag{8.53}$$

8.3.4 Miscellaneous Circuits

Logic Levels

In digital circuitry two states (0, 1) must be represented e. g. by a respective voltage range. For CMOS circuits the two ranges are separated by half the power supply voltage *(V_{DD})*. For a 3 V supply the logic-'0'-state is represented by a voltage level below 1.5 V, a voltage level above 1.5 V corresponds to the logic-'1'-state. Voltage levels near this threshold could cause errors in interpretation. Therefore the output of logic gates should produce a voltage of lower than 10 % of V_{DD} to represent a '0', and a voltage higher than 90 % of V_{DD} to represent a '1' [Hor 89], whereas the input of a logic gate should interpret a voltage level below 30 % of V_{DD} as '0' and a voltage higher than 70 % of V_{DD} as '1'.

Due to the representing voltages the '0' is often referred to as LOW-state, the '1' as HIGH-state.

The operation with the logic states is mathematically described by Boolean logic.

Digital Gates

To negate a logic signal (NOT), an inverter is used as shown in Figure 8.27.

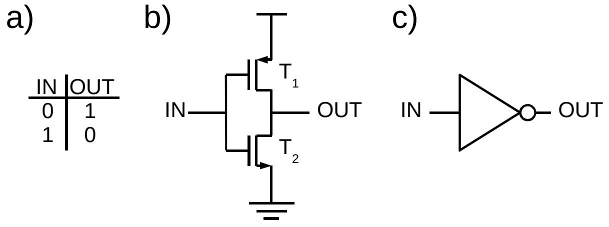

Figure 8.27 CMOS-Inverter: a) the logic table, b) realisation with transistors, c) symbol

The logic table (a) lists all possible input states and their corresponding output results. A CMOS realisation (b) with two complementary transistors and the symbol (c) of an inverter are shown. The circle at the output of the symbol tags its inverting characteristic. Due to the different transconductance parameter *(KP)*, the PMOS T_1 is typically sized between two and three times broader than the NMOS T_2 to achieve the same channel resistance and therefore the same rise- and fall-time. An inverted signal might be written as $\overline{A}$ or $-A$.

To provide the inverted signal only for a certain period, a clocked inverter is used as shown in Figure 8.28.

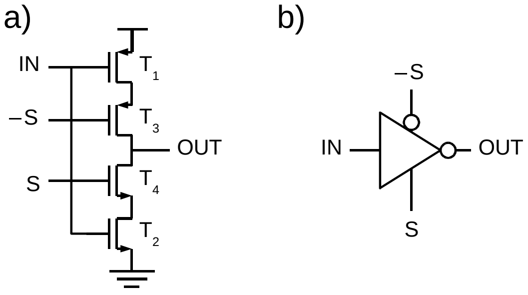

Figure 8.28 Clocked inverter: a) transistor level implementation, b) symbol

The complementary signals S, −S defining the operating state. While S is low (−S high), the transistors T_3 and T_4 are switched off. The output is floating. While S is high (−S low), the transistor $T_{3,\ 4}$ switches the inverter, formed by T_1, T_2 to the output. For this time the output equals the inverted input signal.

The truth table of basic gates with two logic inputs (A, B) are listed in the following table (Table 8.2). An AND checks, if both signals are '1'. The output of an OR is '1', if at least one input is on, whereas the eXclusive OR (XOR) only shows a '1', if exactly one (not both!) input is on.

inputs		outputs					
A	B	$A \cdot B$ (AND)	$A+B$ (OR)	$A \oplus B$ (XOR)	$-(A \cdot B)$ (NAND)	$-(A+B)$ (NOR)	$-(A \oplus B)$ (XNOR)
0	0	0	0	0	1	1	1
0	1	0	1	1	1	0	0
1	0	0	1	1	1	0	0
1	1	1	1	0	0	0	1

Table 8.2 'Truth table' of basic logic gates

All logic-gates exist with inverted outputs, since their transistor-level implementation requires less transistors as shown in Figure 8.29. An AND is implemented as a NAND (NOT AND) with subsequent inverter, the origin of an OR is formed by a NOR (NOT OR).

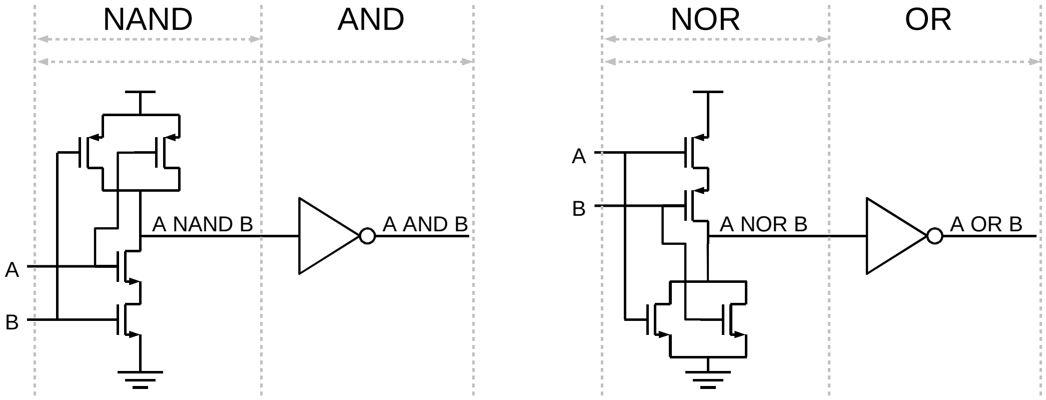

Figure 8.29 Transistor-level implementation of logic-gates

Figure 8.30 shows the symbols of the logic-gates.

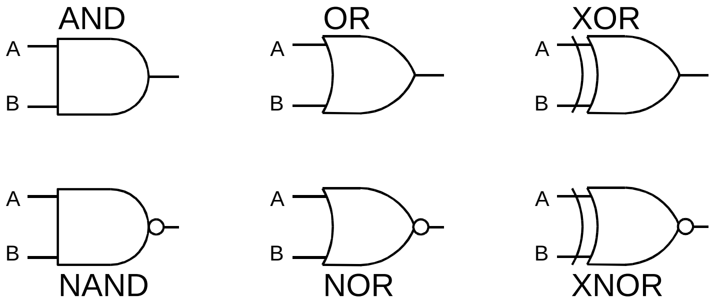

Figure 8.30 Symbols of logic-gates

In the NAND gate, the pull down is realised by two NMOS transistors in series. Whereas in the worst case, the pull up is achieved by one PMOS transistor. In the inverter, the PMOS transistor is designed twice as wide as the NMOS. In the NAND-gate all transistors can have the same size, as the two serial NMOS have about the same resistance as one PMOS.

The NOR gate has two PMOS transistors in series, requiring four times larger PMOS-FETs than NMOS-FETs.

De Morgan[67] laws

$$\begin{aligned}\overline{A\cdot B}&=\overline{A}+\overline{B}\\ \overline{A+B}&=\overline{A}\cdot\overline{B}\end{aligned} \tag{8.54}$$

show how to replace a NAND by an OR and a NOR by an AND. As the NOR requires larger transistors and therefore a larger area, a logic based on NANDs is preferred for high integration.

If the speed and therefore the rise and fall time of logic gates is of no importance, the gates can be designed using minimum transistor dimensions to achieve an area efficient layout.

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[67] Augustus De Morgan: 27.06.1806–18.03.1871

For simplicity the presented gates have only two inputs, which can be easily expanded to the required number of inputs.

Flip-Flops

A second class of problems cannot be solved by forming a combinational function of the inputs alone, but requires knowledge of past inputs as well, e. g. parallel-to-serial converter, counters or arithmetic logic units. This digital memory often is realised with flip-flops. A flip-flop based on NANDs is shown in Figure 8.31.

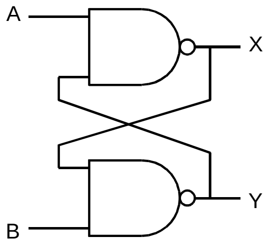

Figure 8.31 Flip-flop ("set-reset"-type)

Assuming both inputs (A, B) are low. The outputs (X, Y) must be high. Changing A to high causes X going low. Now changing B has no effect. By pulling B high before A is high, causes Y going low. The output depends on the chronological order, in which A and B are pulled high. As soon as one of the inputs is high, the outputs are complementary (X=−Y). If both inputs are high, X can be set, by pulling B low (set input). X can be reset by pulling A low (reset input). For this reason the above flip-flop is called RS-flip-flop (reset-set-flip-flop).

To be only sensitive on the input for a certain period, some additional logic has to be implemented as shown in Figure 8.32.

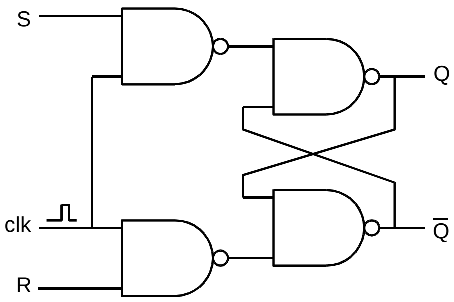

Figure 8.32 Latch

During the high level of the clock signal, the inputs (R, S) control the output: If only one of the inputs is high, the output is set (S=1) or reset (R=1). If both inputs are high, an undetermined state is caused and should be avoided. If both inputs are low, the output state is not changed. This configuration is known as latch.

Another important flip-flop is the edge-triggered delay flip-flop (D-flip-flop) shown in Figure 8.33.

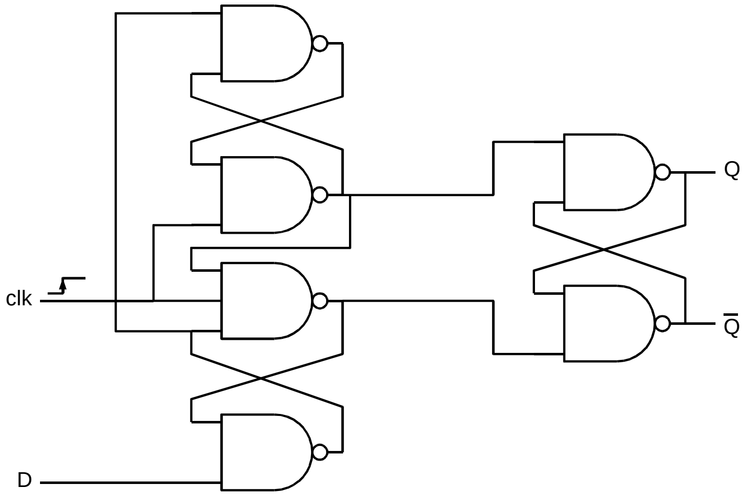

Figure 8.33 Edge-triggered D-flip-flop

The D-input is sampled on the rising edge of a clock-signal. The sampled signal remains at the output even if D is changed. An implementation of this D-flip-flop would require 26 transistors in total: 5×NAND (4 FETs each) with 2 inputs, one NAND with 3 inputs (6 FETs). An implementation with clocked inverters, as shown in Figure 4.33, requires only 16 FETs.

Transmission Gate

A frequently required circuit is an electronic switch to connect an usually analog signal to an input of the subsequent circuitry, e. g. an analog multiplexer to select one out of several signals. As a single transistor cannot perform the transmission of all voltages between ground and the positive supply voltage, a complementary solution is used as shown in Figure 8.34.

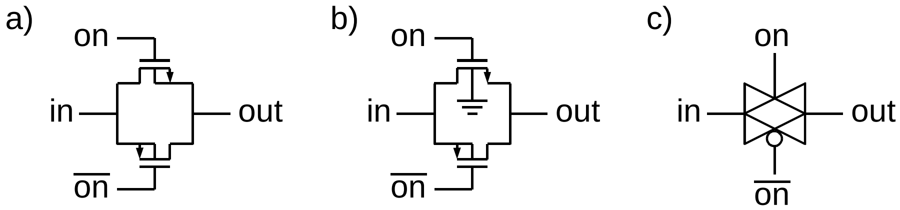

Figure 8.34 Transmission gates: a) ideal realisation in a twin well process, b) realisation in an n-well process, c) logic symbol

To connect input and output of the transmission gate, an 'on'-signal has to be applied at the gate of the NMOS and the inverted signal at the gate of the PMOS.

Analog Multiplexer (MUX)

An analog multiplexer selects one out of 2^N analog signals[68]. The selection is made via N bits, which are decoded to 2^N outputs in the way that a binary input m causes

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[68] MUX with an arbitrary number of input signals can be built. The discussion is limited to simple configurations, which typically offer 2^N inputs.

a high Q_m output while all other outputs are low (binary-to-decimal decoder). The output Q_m is used to connect the analog input in_m via a transmission gate to the analog output.

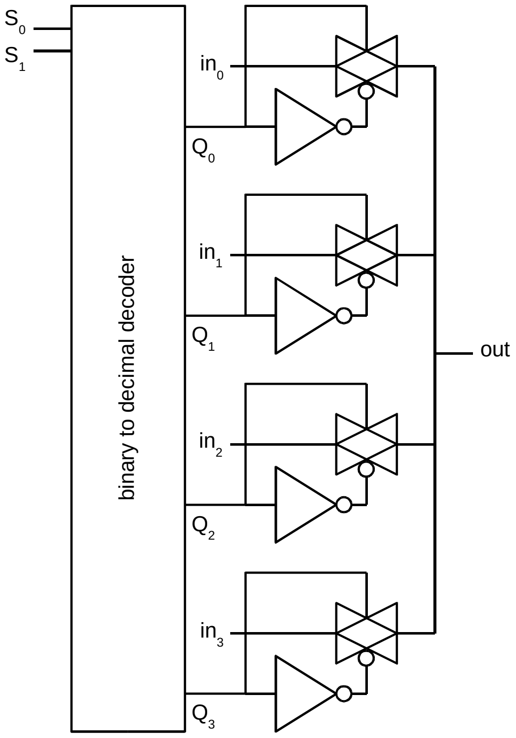

Figure 8.35 A four bit multiplexer

An example of an four bit MUX *(N=2)* is shown Figure 8.35.

Level Shifter

In complex mixed signal[69] chips multiple supply voltages are used in different blocks (e. g. analog/digital supply voltage). To permit a communication between those blocks, a level adaptation must be performed. A simple level shifter is shown in Figure 8.36.

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[69] In a mixed signal environment both analog processing circuits and digital logic is implemented. It is very challenging to avoid cross coupling between both blocks, because proper shielding on the same die is difficult.

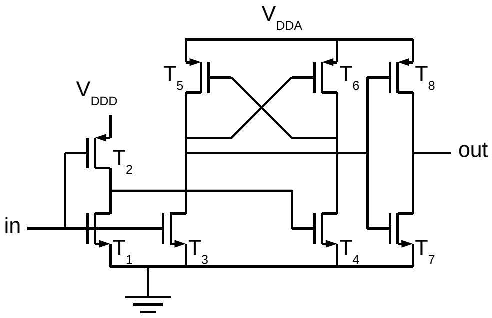

Figure 8.36 Level shifter circuit

Assuming the input 'in' is low. Meanwhile the transistor T_3 is off, the transistor T_4 is switched on via the inverter (T_1, T_2) and pulls the gate of T_5 to ground. Thereby the transistor T_5 is switched on and T_6 off respectively, resulting in a stable state. The output is decoupled from this simple flip-flop via an additional inverter (T_7, T_8). If the input is pulled high, the transistor T_3 begins to pull the gate of T_6 to ground. To achieve this, the transistor T_5 (still on!) must be weaker compared to T_3, which is realised by a long PMOS-transistor. For symmetry the transistors T_5 and T_6 are matched.

8.4 Noise Sources

The term "noise" refers to spontaneous fluctuations of the current passing through, or the voltage developed across, a device. As these fluctuations have different origins, the noise contributions can be subdivided into three types: thermal noise, flicker noise and shot noise.

8.4.1 Thermal Noise or Johnson Noise or White Noise

The basic reasons for this noise are the thermal fluctuations of the electron distribution in a conductor. Therefore thermal noise depends on temperature but not on current flow. It is also called white noise as the spectral noise density is uniformly distributed over all frequencies. The spectral noise voltage density of the thermal noise of a resistor R is given by

$$\overline{v_R^2} = 4\,k\,T\,R \tag{8.55}$$

in which k is the Boltzmann's constant ($1.38 \cdot 10^{-23}$ J/K) and T the absolute temperature. At room temperature a 1 MΩ resistor generates between 1 Hz and 1 GHz a mean voltage of

$$v_{RMS} = \sqrt{\int_1^{10^9} \overline{v_R^2}\, df} = \sqrt{4\,k\,T\,R(10^9 - 1)} \approx 4\,\text{mV} \tag{8.56}$$

Applying the laws of Ohm and Kirchhoff, the thermal noise voltage source in series with a resistor is replaced by a thermal noise current source parallel to a resistor, which in some circuit configurations is advantageous. The spectral noise current density of a resistor is given by

$$\overline{i_R^2}=\frac{\overline{v_R^2}}{R^2}=\frac{4\,k\,T}{R} \tag{8.57}$$

As the thermal noise depends on the temperature, cooling down reduces the thermal noise contribution. This is not the case for shot noise.

For a MOSFET the thermal noise of the channel resistance is calculated [Cha 97] to be

$$\overline{i_d^2}=4\,k\,T\,\gamma\,g_m \tag{8.58}$$

where γ is a very complex function of the basic transistor parameters and bias conditions [Cha 97]. For modern CMOS processes[70] the factor γ is situated between 2/3 and 1. As derived in [Cha 97] $\gamma=2/3$.

Assume that the bandwidth of the output noise of a resistor is limited by means of a capacitor as shown in Figure 8.37.

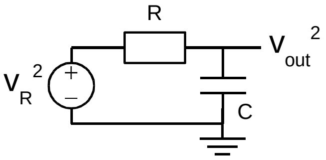

Figure 8.37 Output noise of a resistor R with a subsequent capacitor C

Calculating the rms-noise by integrating the noise power density *($v_R^2=4kTR\ df$)* over all frequencies and taking the transfer function of an RC-filter into account, yields:

$$\overline{v_{out}}=\sqrt{\int_0^\infty 4\,k\,T\,R\left|\frac{1}{1+2\pi\,i\,f\,R\,C}\right|^2 df}=\sqrt{\frac{4\,k\,T\,R}{2\pi\,R\,C}\int_0^\infty\frac{1}{1+x^2}\,dx}=\sqrt{\frac{k\,T}{C}} \tag{8.59}$$

The result is remarkable as it shows that the noise generated by a resistor depends only on its shunt capacitance. This is an important result for the design of sample & hold circuits and peak detectors.

8.4.2 Flicker Noise or 1/f Noise

Flicker noise is found in all active devices, as well as some discrete passive elements such as carbon resistors. The origins of flicker noise are many and diverse, but typically caused by traps associated with contamination and crystal defects [Gra 84]. Flicker noise is always associated with a flow of direct current and shows a spectral density of the form

$$\overline{i^2}=KF\,\frac{I^{af}}{f^{ef}} \tag{8.60}$$

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[70] In modern CMOS processes the gate oxide thickness is in the order of several 10 nm and the substrate doping N_B of about $10^{15}...10^{16}$ cm^{-3}.

The flicker noise coefficient *KF* is a constant for a particular device, *af* is constant in the range 0.5...2 and *ef* is about unity[71].

The conductive channel of the MOSFET is underneath the surface of the silicon. The interface to the gate oxide (SiO_2) causes traps due to the different lattice. Each trapping and detrapping event results in a random telegraph signal corresponding to a Lorentzian spectrum or generation-recombination spectrum. The superposition of such Lorentzians with a proper time constant distribution results in the output flicker noise as modelled in SPICE[72] [Cad 98], [All 87], [Liu 01]:

$$\overline{i_{DS}^2} = \frac{K_f I_{DS}^{af}}{C_{ox} L^2 f^{ef}} \tag{8.61}$$

The mean square current can be reflected to the gate of the MOS device by dividing equation 8.61 by g_m^2 (see equations 8.12 and 8.5):

$$\overline{v_f^2} = \frac{\overline{i_{DS}^2}}{g_m^2} = \frac{K_f I^{af-1}}{2KP\, C_{ox} W L f^{ef}} = \frac{K_f I^{af-1}}{2\mu C_{ox}^2 W L f^{ef}} = \frac{K'_f I^{af-1}}{C_{ox}^2 W L f^{ef}} \quad \text{for}\, K'_f = \frac{K_f}{2\mu} \tag{8.62}$$

Depending on the dimension of K_f either K_f (amperes^{2-af}· farad) or K'_f (coulomb^2/meter^2 for $af=1$) has to be used. If K_f has no unit (e. g. in SPICE), the mean output voltage density is given in V^2/Hz for the current I [A], C_{ox} [F/m^2], W [m], L [m] and f [Hz].

Both the flicker noise coefficient K_f, the flicker noise frequency exponent $ef \approx 1$ and the capacitance per unit area C_{ox} are process parameters. The width W and length L are the effective geometrical dimensions of the MOSFET.

Typical values of the flicker noise coefficient K'_f are given by [Lak 94]:

p-JFET	10^{-33} C^2/cm^2
p-MOSFET	10^{-32} C^2/cm^2
n-MOSFET	$4 \cdot 10^{-31}$ C^2/cm^2

Table 8.3 Flicker noise coefficients

The junction field effect transistor (JFET) has the lowest flicker noise. Considering the flicker noise, an n-MOSFET is worse than a p-MOSFET. In a customary CMOS-process no JFET is available. Therefore, if flicker noise is an issue, a p-MOSFET will be preferred over an n-MOSFET.

8.4.3 Shot Noise

As a result of the discontinuous character of electronic charges the number of charges is subject to fluctuations. Therefore a constant current I_D causes a spectral noise current in a junction diode of

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[71] In the present case *ef* equals unity.

[72] Slight different noise models are used in SPICE depending on the required accuracy. The model is selected by a simulation parameter.

$$\overline{i_D^2} = 2\,q\,I_D \tag{8.63}$$

In the case of a detector readout the leakage current of the detector is a relevant source of shot noise. Equation 8.63 is valid for forward bias current as well as for reverse current. Shot noise does not depend on temperature but only on the current flow.

8.4.4 Additional Noise Sources in MOSFETs

Up to now, the most important noise sources in MOSFETs have been discussed, which are sufficient to predict the noise performance of CMOS circuits in most practical cases. For ultra low noise applications, the mentioned noise sources must be made extremely low by using for instance large transistors and high DC bias levels. Other noise sources could turn out to become important, e. g. the thermal noise associated with the resistive poly-gate, the thermal noise due to the resistive substrate and the shot noise associated with the leakage current of the drain-bulk and source-bulk inverse diodes. For a more detailed discussion, see [Cha 97].

8.5 Data Sheets

Specifications

An overview of the specifications of the three chip versions is given in Table 8.4.

	Ramses 1	Ramses 2	Ramses 3
process	AMS 0.8 µm	AMS 0.6 µm	
metal layers (for routing)	2	3	
poly silicon layers (for capacitors)	2		
chip size [µm × µm] [mm^2]	2380 × 2490 5.93	3881 × 3881 15.1	6600 × 1515.15 10.0
number of pixels (columns × rows)	8 × 8 = 64	32 × 32 = 1024	32 × 2 = 64
pixel size [µm × µm]	150 × 150	100 × 100	200 × 200
number of wire bond pads	51	68	58
diameter of metal bump pad [µm] and passivation opening [µm]	29 15	23 15	53 45
quantity of fets per pixel • NMOS • PMOS	 81 86	 101 103	 330 321
quantity of capacitors per pixel	3	4	16
active elements outside of pixel • NMOS • PMOS • lat. PNP (current reference cell) • diodes (e. g. protection in I/O)	 949 873 – 320	 6969 5957 9 345	 7852 7082 9 333
passive elements outside of pixel • capacitors • resistors	 – 19	 237 8	 236 9

Table 8.4 Overview of the three chip revisions

8.5.1 Ramses 1

Pin Allocation

The pin allocation of the first version of Ramses is given in Table 8.5. The first column gives the pin number on the die, beginning with the ground pin on the left side, which is connected to pin 1 of the JLCC84-package. The connected pins of the JLCC84-package are given in the second column. The successive columns contain the name, the pad type, it's function and a typical operating value.

pin		name	pad	function	typical value
chip	package				
1	1	GND	supply voltage	digital and analog ground	0.0 V
2	2	DISCROUT<47>	digital output	discriminator output of pixel 47	0/VDD
3	3	VDDBUF	supply voltage	power supply for pixel buffer	≥VDDA
4	4	VDDA	supply voltage	analog power supply of CSA	3...5 V
5	5	VCCA	supply voltage	auxiliary analog supply for preamplifier	1.25...2 V
6	6	D	digital input, pull-up	pixel shift register input	0/VDD
7	16	ANALOG IN	analog input, protected	test input for analog pixel buffer in pixel 0	0...VDDA
8	17	SFTESTIN	analog input, protected	input to measure an output buffer (two source follower)	0...VDDA
9	18	SFTESTOUT	analog output (two SF)	analog test output pad	0...VDDA+2 V
10	19	COL<0>	digital output	bit 0 of column address	0/VDD
11	20	COL<1>	digital output	bit 1 of column address	0/VDD
12	21	COL<2>	digital output	bit 2 of column address	0/VDD
13	22	COL<3>	digital output	bit 3 of column address	0/VDD
14	23	HITCOL	digital output	hit column signal	0/VDD
15	24	RCOUT	digital output	shift register output for manual select (EORC)	0/VDD
16	25	ENABLE	digital input, pull-up	enable manual select of pixel	0/VDD
17	26	CLKCOL	digital input, pull-up	clock signal for end-of-column/row logic	0/VDD
18	27	CLKSRIN	digital input, pull-up	clock input for EORC-shift register	0/VDD
19	38	PEAKMON<7>	analog output (two SF)	peak detector output of pixel 7	0...VDDA+2 V
20	39	CRRCMON<7>	analog output (two SF)	CRRC-shaper output of pixel 7	0...VDDA+2 V
21	40	CSAMON<7>	analog output (two SF)	CSA-shaper output of pixel 7	0...VDDA+2 V
22	41	ROW<3>	digital output	bit 3 of row address	0/VDD
23	42	ROW<2>	digital output	bit 2 of row address	0/VDD
24	43	ROW<1>	digital output	bit 1 of row address	0/VDD
25	44	ROW<0>	digital output	bit 0 of row address	0/VDD
26	45	HITROW	digital output	hit row signal	0/VDD
27	46	VCCA	supply voltage	see pin 5	
28	47	VDDA	supply voltage	see pin 4	
29	48	HITBIAS	analog input, protected	current for pull up in hit logic (to VDD)	0...200 µA
30	49	GND	supply voltage	see pin 1	
31	50	VDD	supply voltage	digital and analog supply votlage	3...5 V, VDDA
32	57	IOUTBUF	analog input, protected	bias current of pixel output buffer (to VDDBUF)	0...200 µA
33	58	VBULK	analog input, unprotected	substrate voltage of input transistor in CSA	≥VDDA
34	59	IPEAK	analog input, protected	current for peak detector (to VDD)	0...200 µA
35	60	VIP	analog input, protected	input transistor bias current (to GND)	0...200 µA
36	61	VFEED	analog input, protected	voltage to set the feedback resistance	0...VDDA, 1.4 V
37	62	ITAU	analog input, protected	current to set the peaking time (to GND)	0...200 µA
38	63	VSFN	analog input, protected	current to set the feedback resistance (to GND)	0...200 µA
39	64	VSFP	analog input, protected	load current for output SF in CSA (to VDDSFP)	0...200 µA
40	65	VLOAD	analog input, protected	load current for cascode in CSA (to GND)	0...200 µA
41	66	VTHR	analog input, protected	threshold voltage of discriminator	0...VDDA, 0.93 V
42	67	VDDSFP	supply voltage	supply voltage of CSA source follower	≥VDDA
43	68	ICOMP	analog input, protected	bias current for discriminator (to VDD)	0...200 µA
44	69	ANALOGOUT	analog output (two SF)	analog output of selected pixel	0...VDDA+2 V
45	78	INJECT	analog input, unprotected	test input to inject charge	0...1 V
46	79	Q	digital output	output of the pixel shift register	0/VDD
47	80	SRCLK	digital input, pull-up	clock of the pixel shift register	0/VDD
48	81	CSAOUT<63>	analog output (two SF)	CSA output of pixel 63	0...VDDA+2 V
49	82	CRRCOUT<47>	analog output (two SF)	CRRC-shaper output of pixel 47	0...VDDA+2 V
50	83	CRRCIN<47>	analog input, protected	CRRC-shaper input of pixel 47	0...1 V
51	84	VDD	supply voltage	see pin 31	

Table 8.5 Pin allocation of Ramses 1

Layouts

Figure 8.38 shows the layout of the complete 'Ramses 1'-chip. The chip core is encircled by wire bond pads for simple bonding.

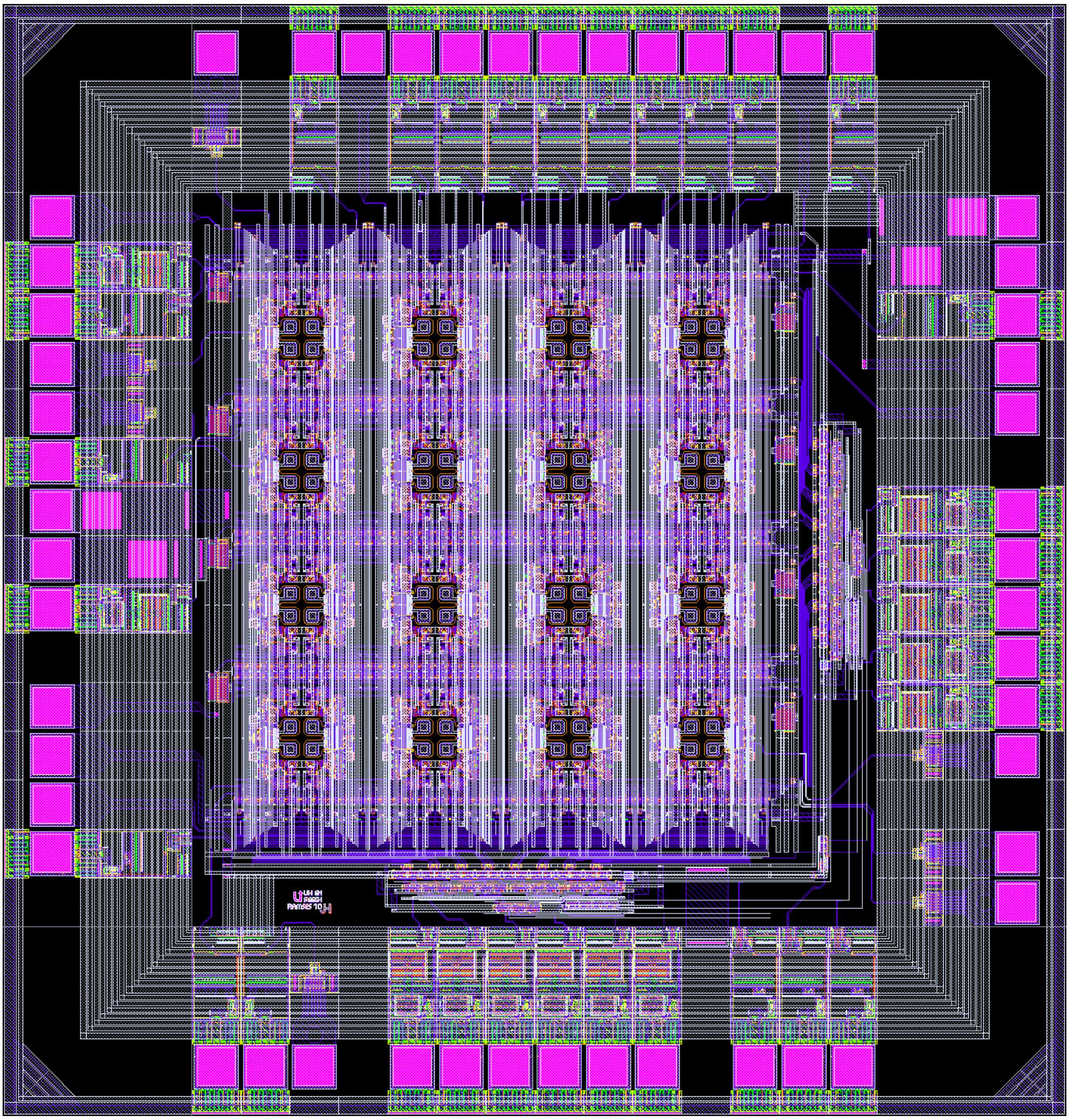

Figure 8.38 Layout of the complete chip 'Ramses 1' (2380 μm × 2490 μm)

An individual pixel is shown in Figure 8.39. Noteworthy are the large areas with no active electronic, which are required for routing as only two metal layers are provided in the AMS 0.8 μm-process.

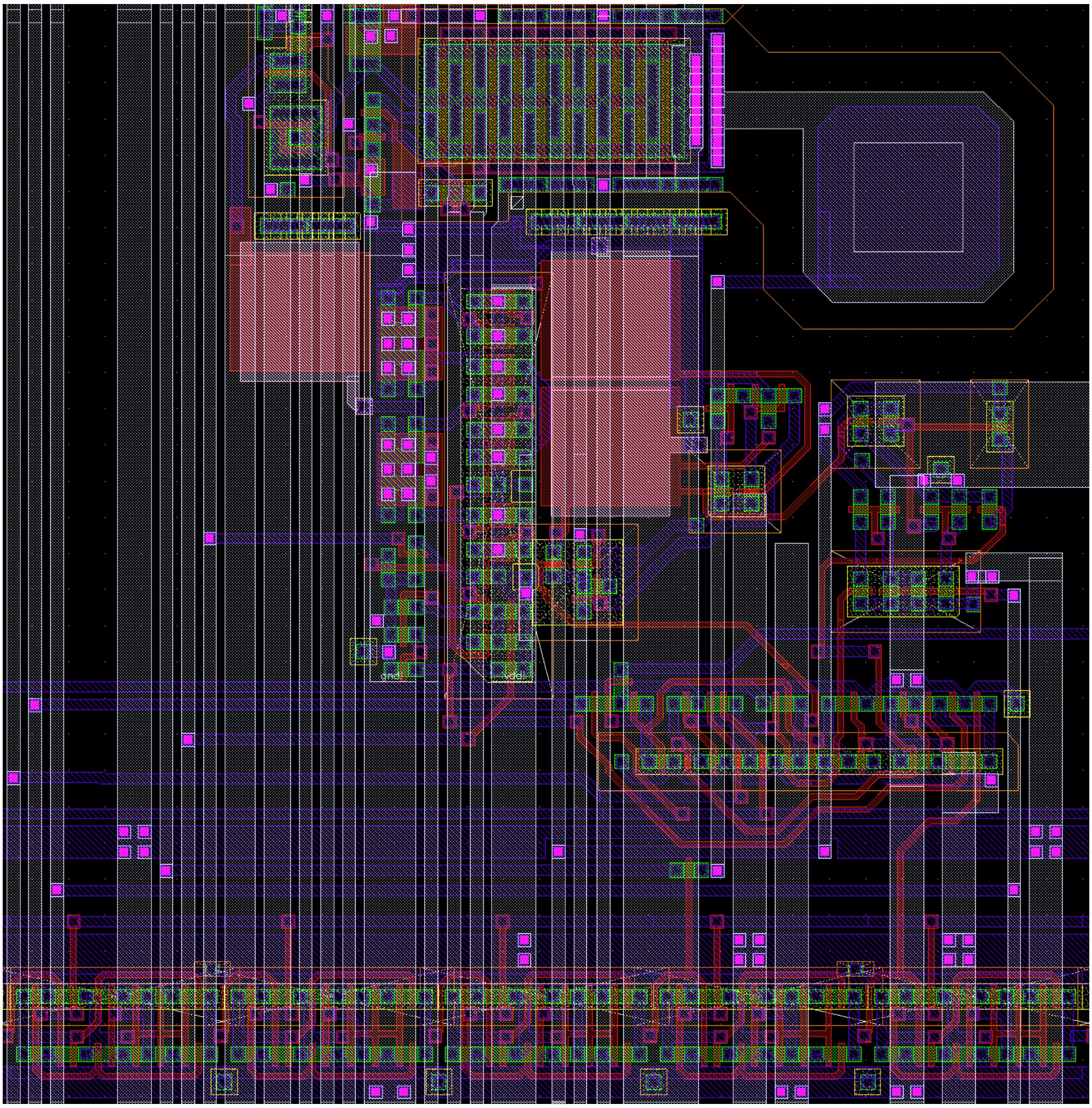

Figure 8.39 A single pixel of 'Ramses 1' (150 µm × 150 µm)

8.5.2 Ramses 2

Pin Allocation

The pin allocation of the second version of Ramses is given in Table 8.6. The first column gives the pin number on the die, beginning with the leftmost pin. The corresponding pins of the JLCC84-package are given in the second column. The successive columns contain the name, the pad type, it's function and a typical operating value.

pin		name	pad	function	typical value
chip	package				
1	7	GNDABUF	supply voltage	analog ground for output buffers and EOC buffers	0.0 V
2	8	TACOUT	analog output	analog TVC-signal	0...VDDABUF
3	9	VDDABUF	supply voltage	positive analog supply for output buffers and EOC buffers	3...5 V
4	10	GNDABUF	supply voltage	connected to pin 1 on chip	
5	11	ANALOGOUT	analog output	analog energy-signal	
6	12	VDDABUF	supply voltage	connected to pin 3 on chip	
7	13	VDDA	supply voltage	analog ground for chip core	0.0 V
8	14	VCCA	supply voltage	auxiliary analog supply for preamplifier	1.25...2.5 V
9	15	GNDA	supply voltage	analog ground for chip core	0.0 V
10	16	VDDD	supply voltage	digital supply for chip core	3...4.5 V
11	17	GNDD	supply voltage	digital ground for chip core	0.0 V
12	18	GNDDBUF	supply voltage	digital ground for digital IO-pads	0.0 V
13	19	COL<4>	digital output	bit 4 of column address	0/VDDDBUF
14	20	COL<3>	digital output	bit 3 of column address	0/VDDDBUF
15	21	COL<2>	digital output	bit 2 of column address	0/VDDDBUF
16	22	COL<1>	digital output	bit 1 of column address	0/VDDDBUF
17	23	COL<0>	digital output	bit 0 of column address	0/VDDDBUF
18	24	HITCOL	digital output	hit column signal	0/VDDDBUF
19	25	D	digital input, pull-up	input for shift registers	0/VDDDBUF
20	26	CLKSEL	digital input, pull-up	clock signal to select shift register	0/VDDDBUF
21	27	CLK	digital input, pull-up	clock signal for selected shift register	0/VDDDBUF
22	28	Q	digital output	output of shift registers	0/VDDDBUF
23	29	LOAD	digital input, pull-up	to load DACs with shift register values	0/VDDDBUF
24	30	VDDDBUF	supply voltage	digital supply for digital IO-pads	3...4.5 V
25	31	ENABLE	digital input, pull-up	to enable the manual selection of a pixel via shift reg.	0/VDDDBUF
26	32	HITBUS	digital output	hitbus signal	0/VDDDBUF
27	33	VCCA	supply voltage	see pin 8	
28	34	VCCA	supply voltage	see pin 8	
29	35	INJECT	analog pad, unprotected	input for injecting electrical test pulses	0...1 V
30	36	VDDA	supply voltage	see pin 7	
31	37	GNDA	supply voltage	see pin 9	
32	38	VCCA	supply voltage	see pin 8	
33	39	VBULK	supply voltage	substrate connections for input transistors of CSAs	≥VDDA
34	40	VREFN	analog pad, unprotected	monitoring/imposing of lower reference voltage for DACs	1.5 V
35	3	A<0>	analog pad, unprotected	monitoring/imposing of DAC<0> current, sfbias	0...200 µA
36	2	A<1>	analog pad, unprotected	monitoring/imposing of DAC<1> current, tbias	0...200 µA
37	1	A<2>	analog pad, unprotected	monitoring/imposing of DAC<2> current, bufbias	0...200 µA
38	84	A<3>	analog pad, unprotected	monitoring/imposing of DAC<3> current, peakbias	0...200 µA
39	83	A<4>	analog pad, unprotected	monitoring/imposing of DAC<4> current, vfeed	0...200 µA
40	82	A<5>	analog pad, unprotected	monitoring/imposing of DAC<5> current, vfeedadj	0...200 µA
41	81	A<6>	analog pad, unprotected	monitoring/imposing of DAC<6> current, vtau	0...200 µA
42	80	A<7>	analog pad, unprotected	monitoring/imposing of DAC<7> current, vthr	0...200 µA
43	79	A<8>	analog pad, unprotected	monitoring/imposing of DAC<8> current, discbias	0...200 µA
44	78	A<9>	analog pad, unprotected	monitoring/imposing of DAC<9> current, iload	0...200 µA
45	77	A<10>	analog pad, unprotected	monitoring/imposing of DAC<10> current, inpbias	0...200 µA
46	76	A<11>	analog pad, unprotected	monitoring/imposing of DAC<11> current, icommonS	0...200 µA
47	75	A<12>	analog pad, unprotected	monitoring/imposing of DAC<12> current, icombias	0...200 µA
48	74	A<13>	analog pad, unprotected	monitoring/imposing of DAC<13> current, hitbias	0...200 µA
49	73	A<14>	analog pad, unprotected	monitoring/imposing of DAC<14> current, hit-busbias	0...200 µA
50	72	A<15>	analog pad, unprotected	monitoring/imposing of DAC<15> current, no connection	0...200 µA
51	41	ROW<4>	digital output	bit 4 of row address	0/VDDDBUF
52	42	ROW<3>	digital output	bit 3 of row address	0/VDDDBUF
53	43	ROW<2>	digital output	bit 2 of row address	0/VDDDBUF
54	44	ROW<1>	digital output	bit 1 of row address	0/VDDDBUF
55	45	ROW<0>	digital output	bit 0 of row address	0/VDDDBUF
56	46	HITROW	digital output	hit row signal	0/VDDDBUF
57	47	GNDDBUF	supply voltage	see pin 12	
58	48	VDDDBUF	supply voltage	see pin 24	
59	49	GNDD	supply voltage	see pin 11	
60	50	VDDD	supply voltage	see pin 10	
61	51	GNDA	supply voltage	see pin 9	
62	52	VDDA	supply voltage	see pin 7	
63	53	GNDABUF	supply voltage	analog ground for output buffer 'DEBUG2OUT'	0.0 V
64	54	DEBUG2OUT	analog output	second analog debug output (8 signals via MUX)	0...VDDABUF
65	55	VDDABUF	supply voltage	positive analog supply for output buffer 'DEBUG2OUT'	3...5 V
66	56	GNDABUF	supply voltage	analog ground for output buffer 'DEBUG1OUT'	0.0 V
67	57	DEBUG1OUT	analog output	first analog debug output (8 signals via MUX)	0...VDDABUF
68	58	VDDABUF	supply voltage	positive analog supply for output buffer 'DEBUG1OUT'	3...5 V

Table 8.6 Pin allocation of Ramses 2

Layouts

Figure 8.40 shows the layout of the complete 'Ramses 2'-chip. The bond pads are arranged only at two sides of the pixel matrix to allow an almost seamless formation of four chips in a square.

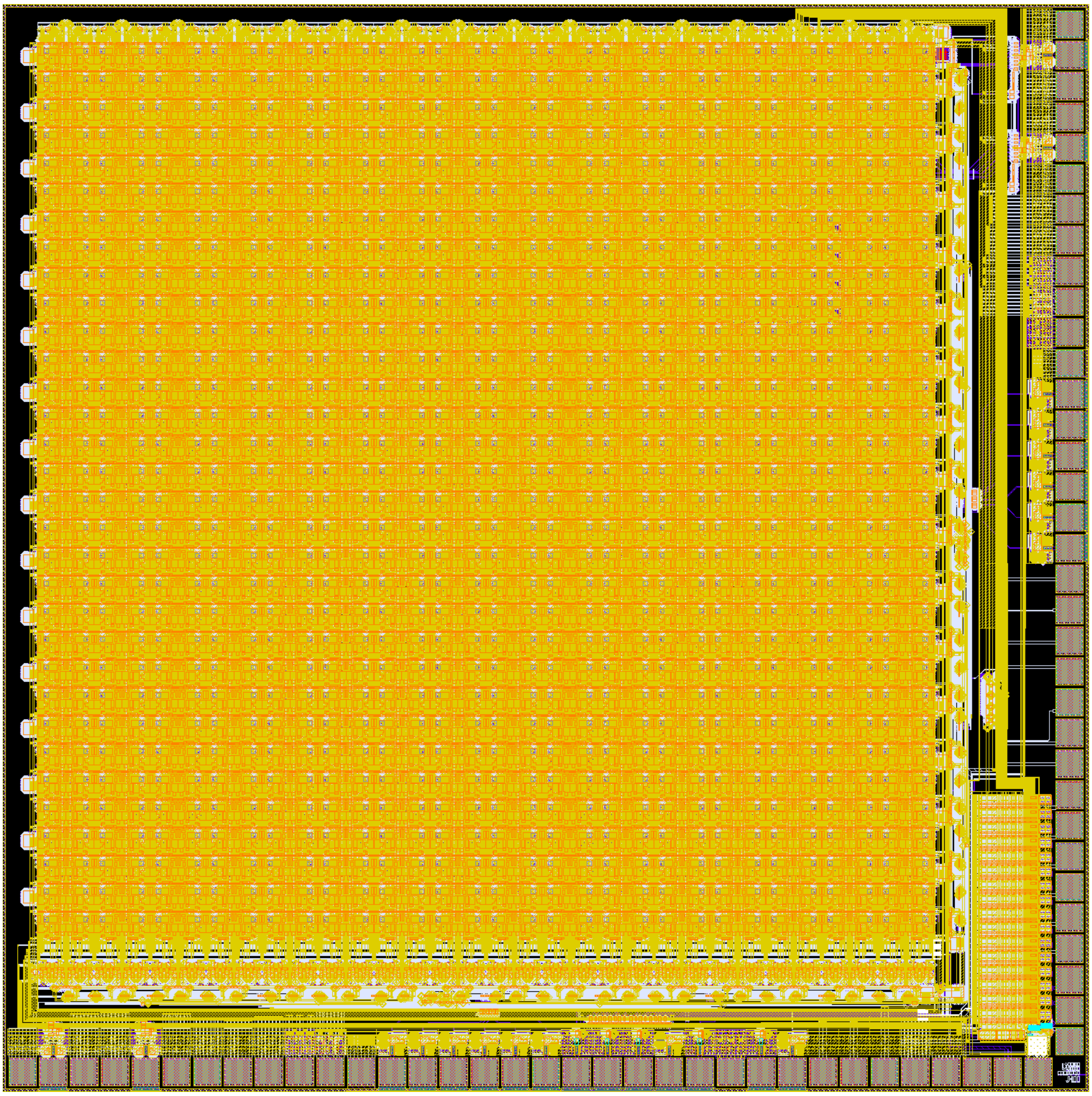

Figure 8.40 Layout of the complete chip 'Ramses 2' (3881 µm × 3881 µm)

An individual pixel is shown in Figure 8.41. The third metal layer permits a very compact layout.

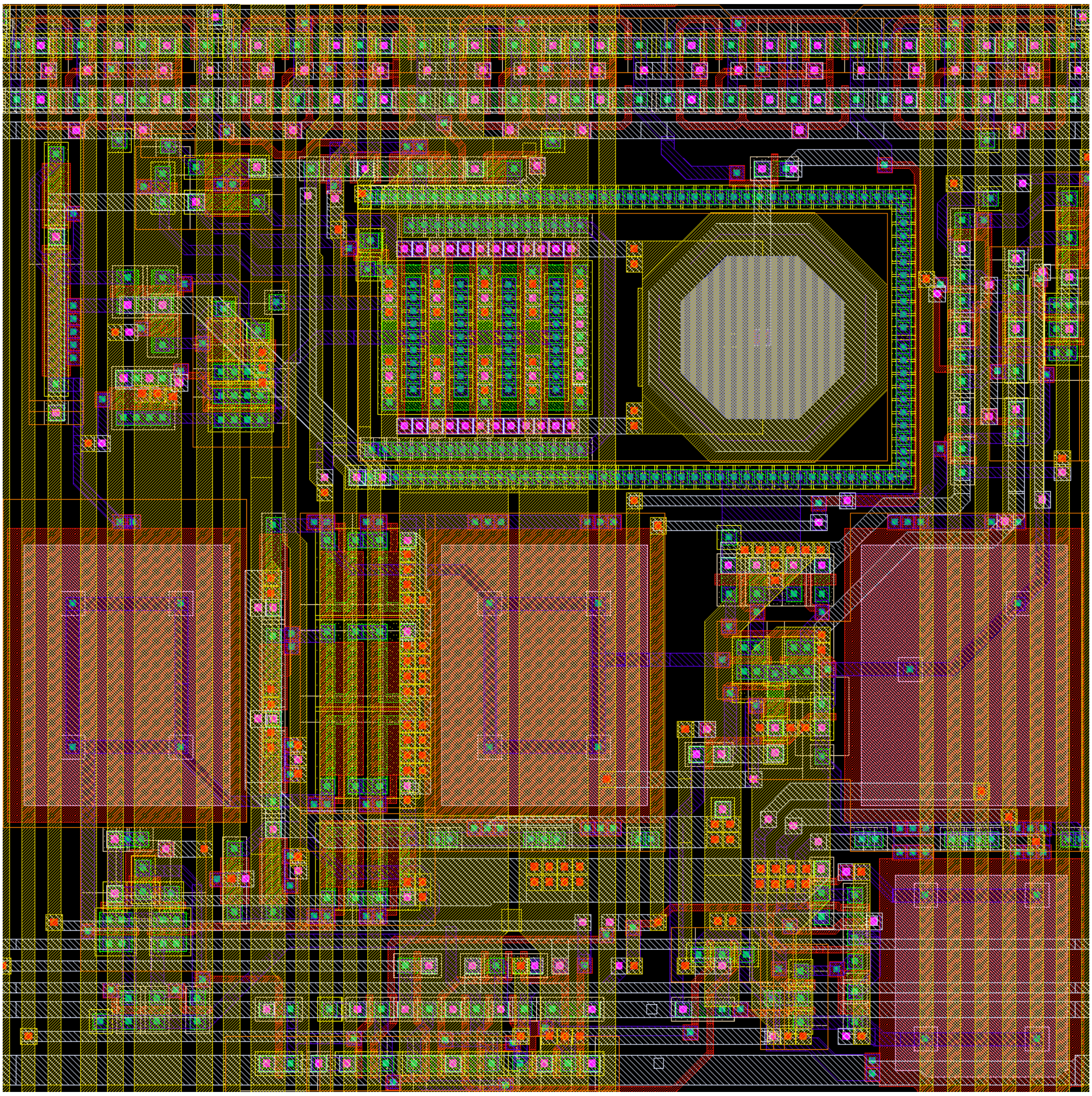

Figure 8.41 A single pixel of 'Ramses 2' (100 µm × 100 µm)

8.5.3 Ramses 3

Pin Allocation

The pin allocation of the third version of Ramses is given in Table 8.7. The first column gives the pin number on the die, beginning with the leftmost pad. In the second column the pin number of the JLCC84-package is given, if the chip is bonded to the package. In the case of a direct mounting on a hybrid board, the pins are given in the third column: The pins are labelled beginning with the leftmost pin. The top (T) and bottom (B) side correspond to the assembly side and the soldering side respectively. The name of the pin in the schematic is specified in the fourth column. In the following fifth column the pad type is given. A short description of the function is itemised in the sixth column. The last column lists typical operating values.

pin			name	pad	function	typical value
chip	package	hybrid				
1	72	1 B	GNDABUF	supply voltage	analog ground for output buffers and EOC buffers	0.0 V
2	73	2 B	ANALOG OUT 1	analog output	output of analog buffer 1	0...VDDABUF
3	74	3 B	VDDABUF	supply voltage	positive analog supply for output- and EOC buffers	3...5 V
4	56	4 B	GNDABUF	supply voltage	connected to pin 1 on chip	
5	55	5 B	ANALOG OUT 2	analog output	output of analog buffer 2	
6	54	6 B	VDDABUF	supply voltage	connected to pin 3 on chip	
7	53	27 B	GND	supply voltage	substrate connections for NMOSFETs	0.0 V
8	52	1 T	GNDA	supply voltage	analog ground for chip core	0.0 V
9	51	2 T	VCCA	supply voltage	auxiliary analog supply for preamplifier	1.25...2.5 V
10	50	3 T	VBULK	supply voltage	substrate connections for input transistors of CSA	≥VDDA
11	49	4 T	VDDA	supply voltage	analog supply for chip core	3...4.5 V
12	75		VDDA	supply voltage	see pin 11	
13	76	5 T	INJECT	analog input, unprotected	input for injecting electrical test pulses	0...1 V
14	77		VDDA	supply voltage	see pin 11	
15	78	7 T	IMON0<0>	analog input/output	multiplexer in-/output for DAC, channel 1	0...200 µA
16	79	28 B	IMON0<1>	analog input/output	multiplexer in-/output for DAC, channel 1	0...200 µA
17	80	8 T	IMON1<0>	analog input/output	multiplexer in-/output for DAC, channel 2	0...200 µA
18	81	9 T	IMON1<1>	analog input/output	multiplexer in-/output for DAC, channel 2	0...200 µA
19	82	10 T	GNDD	supply voltage	digital ground for chip core	0.0 V
20	83	12 T	LOAD	digital input, pull-up	to load DACs with shift register values	0/VDDD
21	84	9 B	D	digital input, pull-up	input for shift registers	0/VDDD
22	48	23 B	CLKSEL	digital input, pull-up	clock signal to select shift register	0/VDDD
23	47	13 T	CLK	digital input, pull-down	clock signal for selected shift register	0/VDDD
24	46	19 T	GNDDBUF	supply voltage	digital ground for digital in-/output pads	0.0 V
25	45	15 T	Q	digital output	output of shift registers	0/VDDDBUF
26	44	10 B	VDDDBUF	supply voltage	supply for digital in-/output pads	≥VDDD
27	1	19 B	VDDD	supply voltage	digital supply for chip core	1.25...5 V
28	2	20 B	VTHRADJEN	digital input, pull-down	to enable analog threshold adjustment of pixel	0/VDDD
29	43		GND	supply voltage	see pin 7	
30	42		GNDA	supply voltage	see pin 8	
31	41		VCCA	supply voltage	see pin 9	
32	40		VBULK	supply voltage	see pin 10	
33	39		VDDA	supply voltage	see pin 11	
34	3	21 B	VTHRSF	analog input	analog threshold for discriminator	0...VDDA
35	38		GNDDBUF	supply voltage	see pin 24	
36	4	20 T	HITCOL<0>	digital output	bit 0 of column address	0/VDDDBUF
37	5	22 B	HITCOL<1>	digital output	bit 1 of column address	0/VDDDBUF
38	6	24 B	HITCOL<2>	digital output	bit 2 of column address	0/VDDDBUF
39	7	25 B	HITCOL<3>	digital output	bit 3 of column address	0/VDDDBUF
40	8	26 B	HITCOL<4>	digital output	bit 4 of column address	0/VDDDBUF
41	9	7 B	HITCOL<5>	digital output	hit column signal	0/VDDDBUF
42	37	8 B	VDDDBUF	supply voltage	see pin 26	
43	10	21 T	HITBUS	digital output	hit-bus signal	0/VDDDBUF
44	11	22 T	ENABLE	digital input, pull-down	to enable the manual selection of a pixel via shift register	0/VDDD
45	36	23 T	GNDDBUF	supply voltage	see pin 24	
46			HITROW<0>	digital output	bit 0 of row address	0/VDDDBUF
47			HITROW<1>	digital output	bit 1 of row address	0/VDDDBUF
48			HITROW<2>	digital output	bit 2 of row address	0/VDDDBUF
49			HITROW<3>	digital output	bit 3 of row address	0/VDDDBUF
50	12	24 T	HITROW<4>	digital output	bit 4 of row address	0/VDDDBUF
51	17	25 T	HITROW<5>	digital output	hit row signal	0/VDDDBUF
52	35	26 T	VDDDBUF	supply voltage	see pin 26	
53	18	27 T	GUARD	supply voltage	connection to the detector guard ring via bump bonds	0.0 V
54	34	28 T	GND	supply voltage	see pin 7	
55	33	29 T	GNDA	supply voltage	see pin 8	
56	32	30 T	VCCA	supply voltage	see pin 9	
57	31	29 B	VBULK	supply voltage	see pin 10	
58	30	30 B	VDDA	supply voltage	see pin 11	

Table 8.7 Pin allocation of Ramses 3

Layouts

Figure 8.42 shows the layout of the complete 'Ramses 3'-chip. As the detector contains guard rings, the detector is significant larger than the pixel matrix. Therefore the distance between wire bond pads and bump bond pads has to be at least 1 mm. Wire bond pads are only located on one side of the chip to reduce die size as the distance to the bump bond pads must be obeyed. A seamless formation of several chips is also possible.

Figure 8.42 Layout of the complete chip 'Ramses 3' (6600 µm × 1515 µm)

An individual pixel is shown in Figure 8.43. The bump bond pad was enlarged for gold stud bonding.

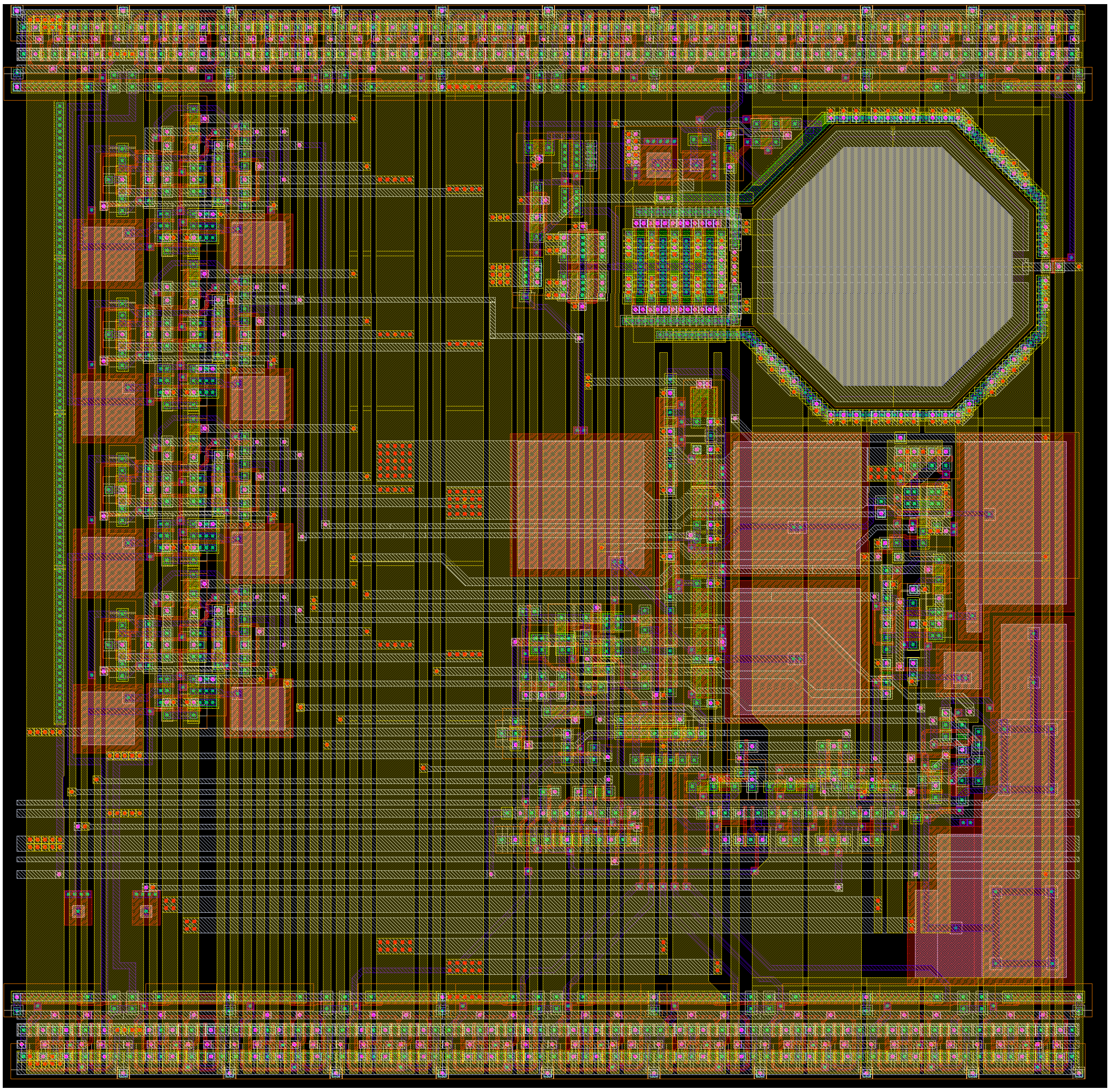

Figure 8.43 A single pixel of 'Ramses 3' (200 µm × 200 µm)

8.6 Physical Constants

name	symbol	value	units
vacuum dielectric constant	ε_0	8.85	aF/µm
silicon dielectric constant	$\varepsilon_{\mathrm{Si}}$	11.7 ε_0	aF/µm
SiO_2 dielectric constant	$\varepsilon_{\mathrm{ox}}$	3.97 ε_0	aF/µm
Boltzmann's constant	k	$1.38 \cdot 10^{-23}$	J/K
mass density of silicon	ρ	2.328	g/cm^3
radioactivity	Ci	$3.7 \cdot 10^{10}$	Bq

Table 8.8 Physical constants

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